#### INFN - Istituto Nazionale di Fisica Nucleare Sezione di Torino

#### A 64-channel wide dynamic range charge measurement ASIC for strip and pixel ionization detectors

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#### Outline



- Application: hadrontherapy
- 1<sup>st</sup> generation ASIC architecture
- Test results
- 2<sup>nd</sup> generation ASIC
- Test results
- Conclusions

#### Hadrontherapy





## **Applications**



#### Two applications :

- beam calibration : a stack of strip segmented ionization detectors interleaved by passive material is used to measure the beam profile before treatment
- beam monitoring : a pixel ionization chamber is used to monitor the hadron beam during patient irradiation
- Both the dose deposited by the beam on the target tissue and the dose on the surrounding tissues has to be measured.
- A very dynamic range, of the order of 10<sup>3</sup>, is required

#### The detectors





The strip detector ( "Magic Cube" )

#### The pixel detector



#### Architecture





#### Waveforms





## Charge subtraction





#### ASIC architecture





## Charge quantum @ 600fC



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### Distribution @ 600fC









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### Linearity – 1a



Chip n. 2 Channel n. 1  $\Delta V = 3 V$ Qc = 610.1 fC Input range : 50 pA ÷ 3  $\mu$ A

The relative deviation is better than .6 %



### Linearity – 2a



Chip n. 2 Channel n. 1  $\Delta V = 500 \text{ mV}$ Qc = 102.2 fC Input range : 50 pA ÷ 500 nA

The relative deviation is better than 1 %



#### Pedestals & test mode





#### Radiation Tolerance





### Application







#### New ASIC





#### Waveforms





#### Subtraction scheme





#### Charge quantum @ 50fC



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#### Distribution @ 50fC







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#### Distribution @ 150fC









Charge quantum (fC)

Gianni Mazza

352.0 ⊑

350.0

348.0

346.0

344.0

342.0

340.0

338.0

336.0

334.0

332.0

330.0

328 326

322

320.0

318.0

316.0

314.0

0

5

10

of entries

ż

zza

Charge quantum (fC)





## Charge quantum



	Negative input current			Positive input current		
$Q_{th}(fC)$	Q <sub>meas</sub> (fC)	r.m.s (fC)	r.m.s (%)	Q <sub>meas</sub> (fC)	r.m.s (fC)	r.m.s (%)
50	42.86	1.42	3.31	45.44	1.42	3.13
100	86.84	1.67	1.92	89.42	1.50	1.68
150	131.06	1.81	1.38	133.68	1.72	1.29
200	189.39	2.07	1.09	192.20	1.92	1.00
250	233.89	2.47	1.06	236.71	2.16	0.91
300	277.70	2.65	0.95	280.65	2.43	0.87
350	322.17	2.84	0.88	325.18	2.74	0.84

# Linearity @ 150 fC - 1



Chip n. 1 Channel n. 15 Negative currents Qc = 132.98 fC Input range : 500 pA ÷ 2.5  $\mu$ A



The relative deviation is around 2%



# Linearity @ 150 fC - 2



Chip n. 1 Channel n. 15 Positive currents Qc = 132.80 fCInput range :  $500 \text{ pA} \div 2.5 \mu\text{A}$ 



The relative deviation is around 2.2 %



## Linearity @350 fC - 1



Chip n. 1 Channel n. 15 Negative currents Qc = 325.73 fC Input range : 500 pA  $\div$  6.5  $\mu$ A



The relative deviation is below 1.7 %





#### Linearity – 350 fC - 2

Chip n. 1 Channel n. 15 Positive currents Qc = 325.86 fCInput range :  $500 \text{ pA} \div 6.5 \mu\text{A}$ 



The relative deviation is around 2.5 %



#### Pedestal





## Comparison



Technology	CMOS 0.8 µm	CMOS 0.35 µm
Die size	6x7 mm <sup>2</sup>	$5.4 \text{x} 4.5 \text{ mm}^2$
N. of channels	64	64
Cint	600 fF	600fF
Q <sub>min</sub>	100 fC	50 fC
Q <sub>max</sub>	1 pC	1.155 pC
Csub	200 fF	$50 \text{ fF} \rightarrow 300 \text{ fF}$
N. of bit of the counter	16	32
Input current	unipolar	bipolar
Max clock frequency	20 MHz	100 MHz
Max I-f converter frequency	5 MHz	20 MHz

#### Conclusions



- A 64-channel ASIC for the readout of strip and pixel ionization detectors has been designed in a 0.8 µm CMOS technology and tested.
- The charge balancing integration technique allows for a dynamic range in excess of 10<sup>3</sup> with a nonlinearity of less than 1%
- The ASIC is currently used in a commercial product in the framework of a technology transfer program
- A 2<sup>nd</sup> generation ASIC in 0.35 µm technology with bipolar input capability and improved performances has been designed and tested



# Spare slides



- \* Tera 01 : first prototype with 14 channels in CMOS 1.2 μm (1996)
- \* Tera 02-03 : 64 channels chips with asynchronous logic and 20/16 bits counters in CMOS 0.8 μm (1997-98)
- \* Tera 04 : 64 channels chip with synchronous logic and 16 bit counter (1999) *not working*... :-(
- \* Tera 05-06 : same as version 4 after bug correction and mass production for IBA (2000-02)
- Tera 07 : upgrade with bipolar input capability and digital charge quantum selection in CMOS 0.35 μm (2004-05)

#### Temperature variation







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#### Distribution @ 100fC





# Charge quantum @ 200fC







#### Distribution @ 200fC





# Charge quantum @ 250fC



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#### Distribution @ 250fC







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Negative current Positive current 302.0 302.0 300.0 300.0 298.0 298.0 296.0 296.0 294.0 294.0 Charge quantum (fC) Charge quantum (fC) 292.0 292.0 290.0 290.0 288.0 288.0 286.0 286.0 284.0 284.0 282.0 282. 280.0 280 278.0 278.0 276.0 276.0 274.0 274.0 272.0 272.0 270.0 270.0 25 30 35 40 45 50 55 60 5 15 20 25 30 35 40 45 50 55 60 5 10 15 20 10 0 0 Channel number Channel number 20 chips  $\Delta V$ Itest = 100 nAcapsel = 110



