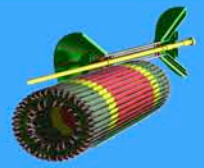
# ALICE Silicon Pixel Detector (SPD)

*Alexander Kluge*
*CERN-PH/ED*

**FEE 2006**
**CERN, May 17-20, 2006**

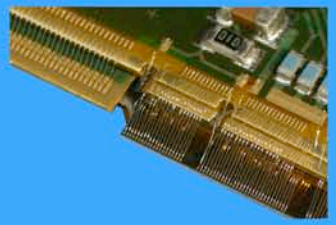
# Overview

- **ALICE SPD**
  - Detector, Specification and Challenge

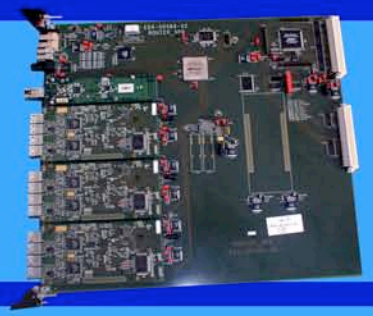


- **Electronics Architecture & On-detector Electronics**

- **Electronics Integration**

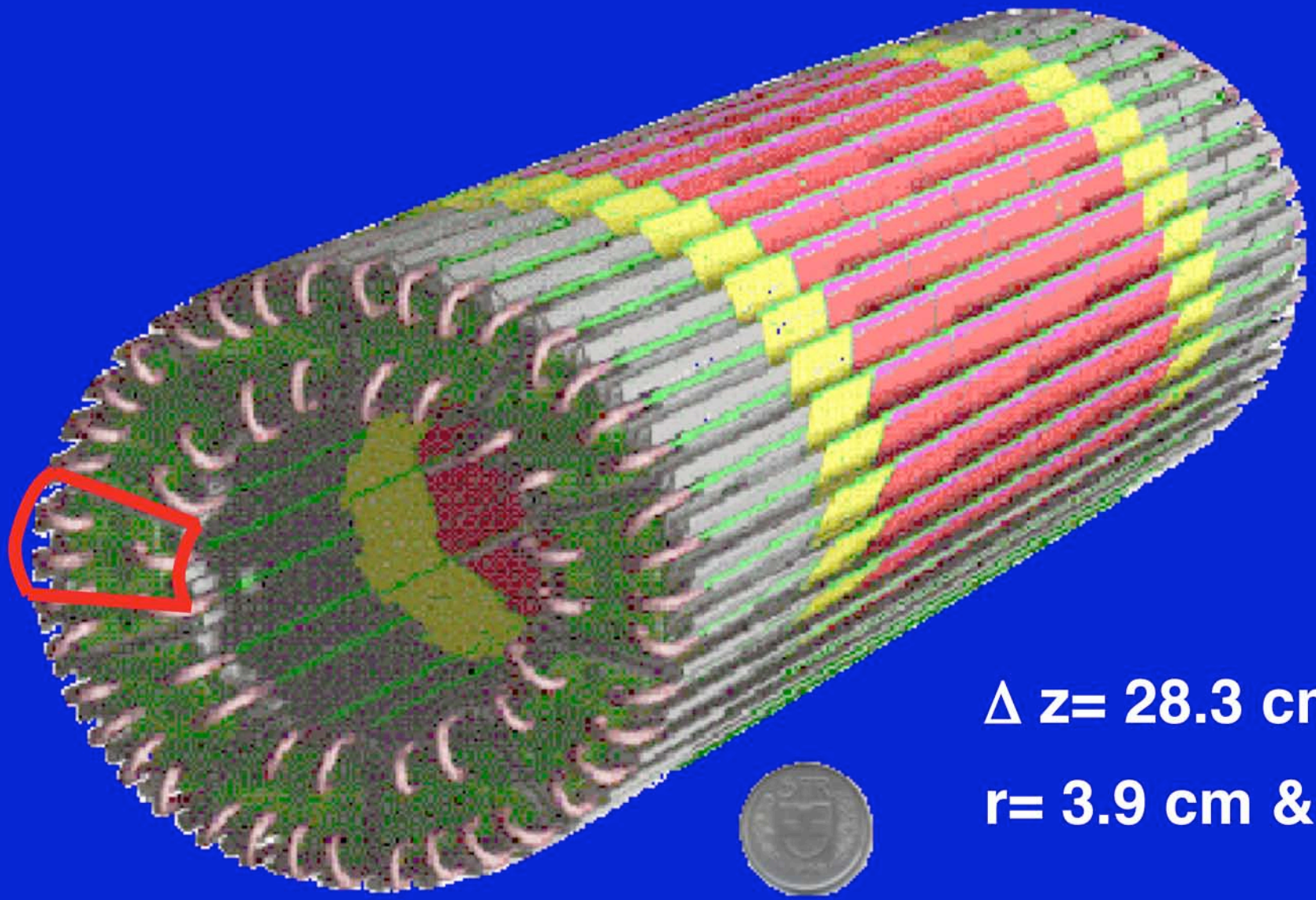


- **Off detector electronics & Infrastructure & Pixel trigger**



- **Conclusion**

# The SPD Detector



Δ z= 28.3 cm

r= 3.9 cm & 7.6 cm

# SPD half stave

On detector
Readout electronics

1 ladder

1 ladder

10 readout chips

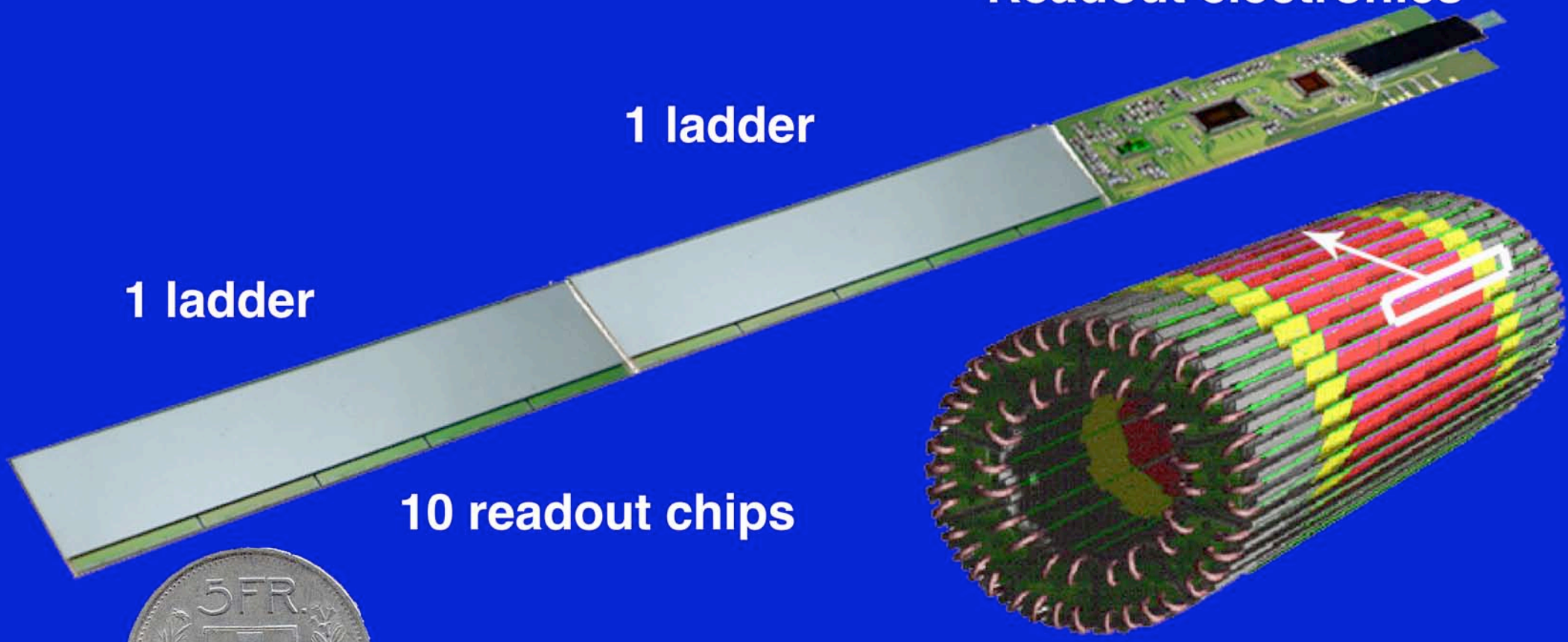



Image:INFN(Padova)

# System parameters

# System Parameters

- ~ 10 million channels, 120 detector modules
- L1 after 6 μs, L1 rate 1 kHz
- L2 after 100 μs, L2 rate 40 - 800Hz
- Readout upon L2
  - ~ 1 GB/s raw data
- Readout time: 256 μs
- Radiation: 250 krad
  neutron flux: $3 \times 10^{11} cm^{-2}$ (10y)
- Material budget: 1% per layer

# The challenge

physical size = 200 mm x 15 mm x 2 mm

material budget = 1% $X_0$ -> no copper

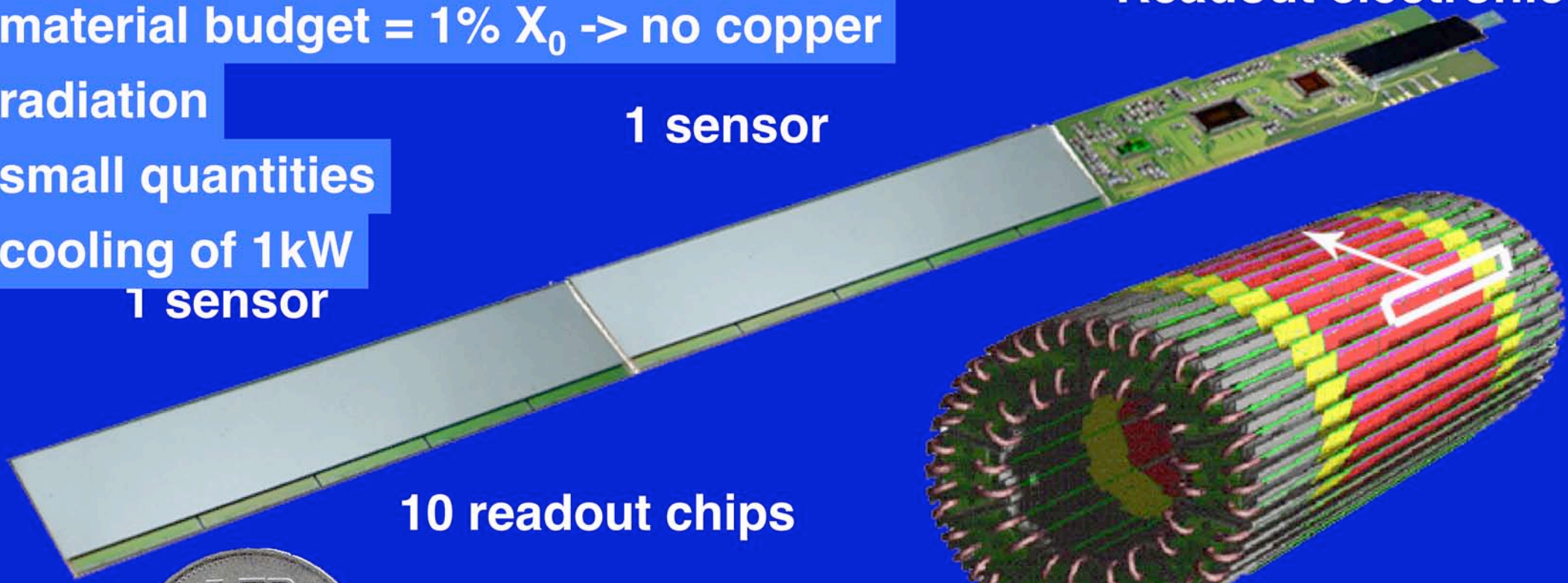
radiation

small quantities

cooling of 1kW

On detector
Readout electronics

1 sensor



1 sensor

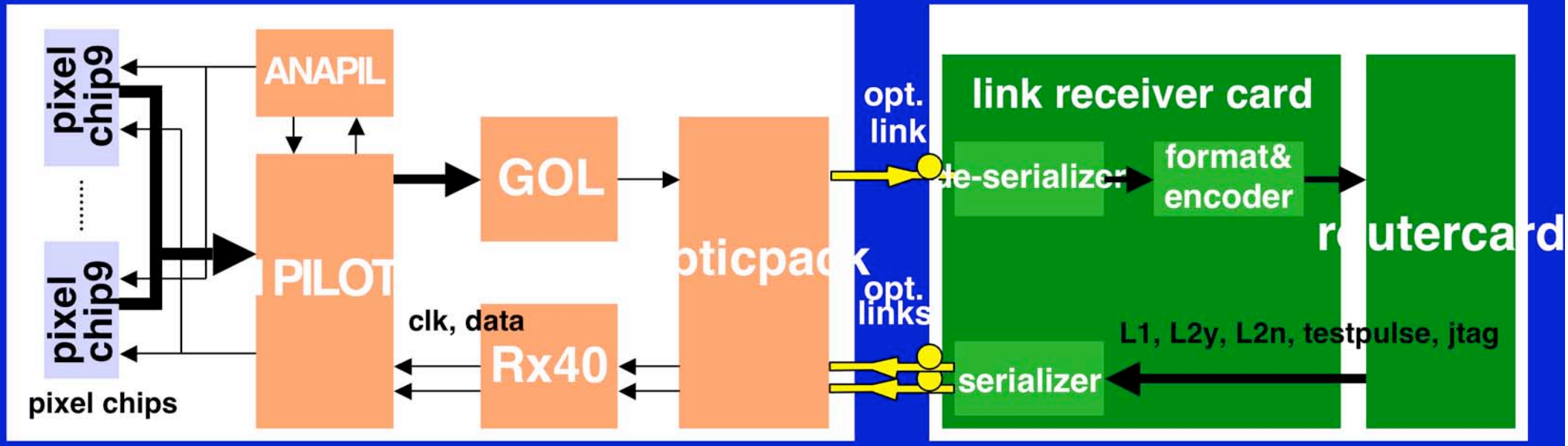
10 readout chips




Image:INFN(Padova)

# Read-out architecture

# Pixel read out system



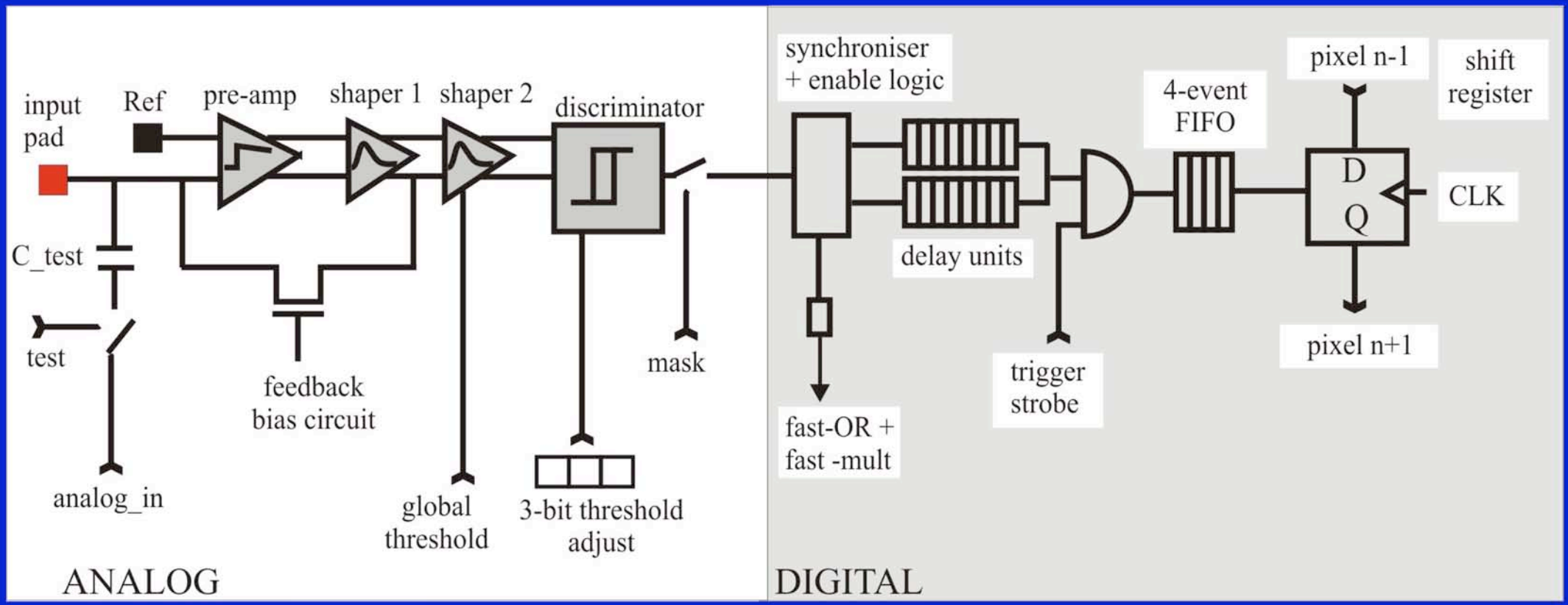
# On detector electronics elements

- Pixel chip & sensors
- Multi chip module + ASICs
- Al Multi-layer kapton cables (Bus)

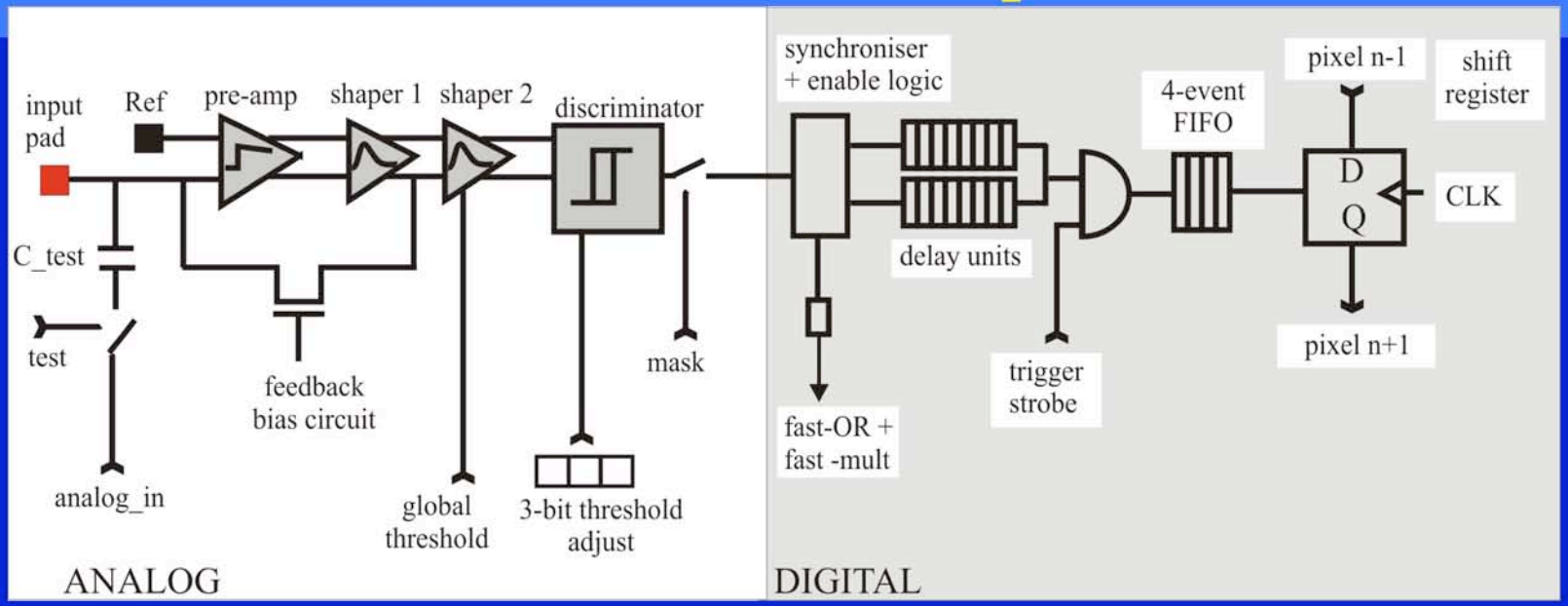
# On detector electronics elements

- **Pixel chip & sensors**
- **Multi chip module + ASICs**
- **Al Multi-layer kapton cables (Bus)**

# Pixel chip

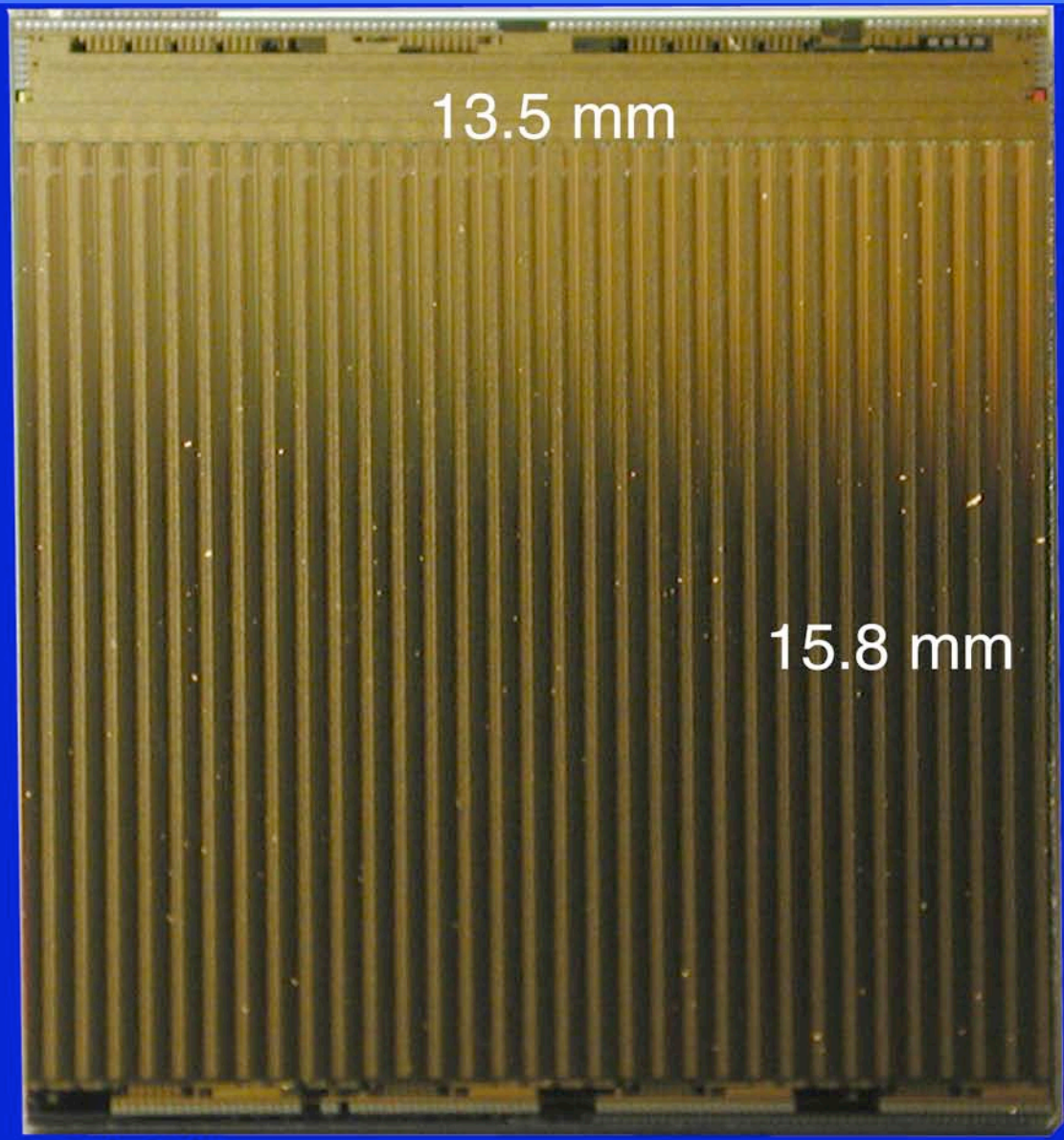

input pad
Ref
pre-amp
shaper 1
shaper 2
discriminator
C_test
test
feedback bias circuit
analog_in
global threshold
3-bit threshold adjust
mask
ANALOG
synchroniser + enable logic
delay units
fast-OR + fast -mult
trigger strobe
4-event FIFO
pixel n-1
shift register
D
Q
CLK
pixel n+1
DIGITAL

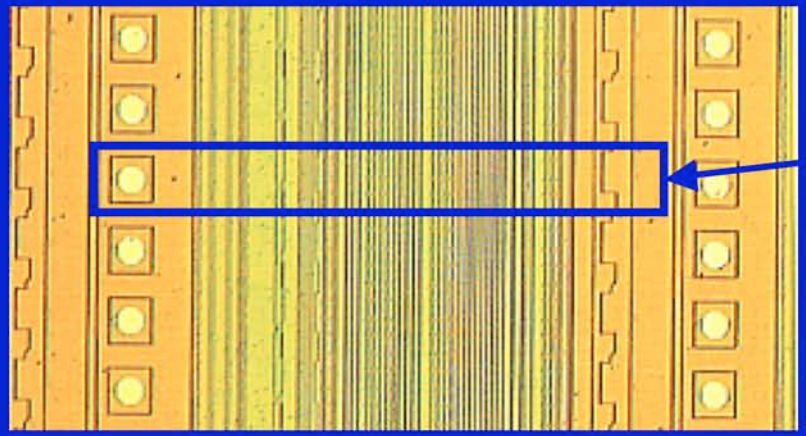
# Pixel chip



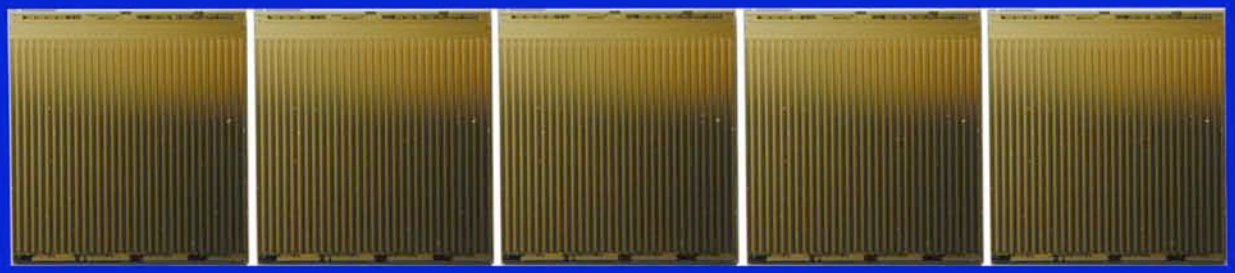

- pixel size 425$\mu$m x 50 $\mu$m
- pixel matrix 256 x 32 = 8192
- differential front end
- 150 $e^-$ noise, 100$\mu$W/pixel
- binary synchronous read-out
- read-out on 32 bit parallel bus @ 10 MHz
- configuration loading via JTAG
- I/O with GTL logic
- 5 bit reg./pixel & 42 DACs for configuration
- external analog bias inputs

# Pixel chip



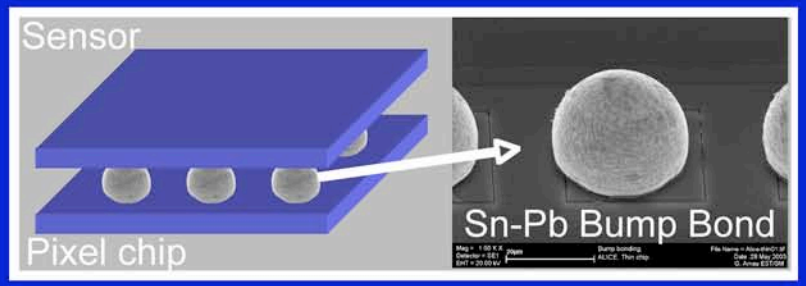



# Sensor & pixel chips



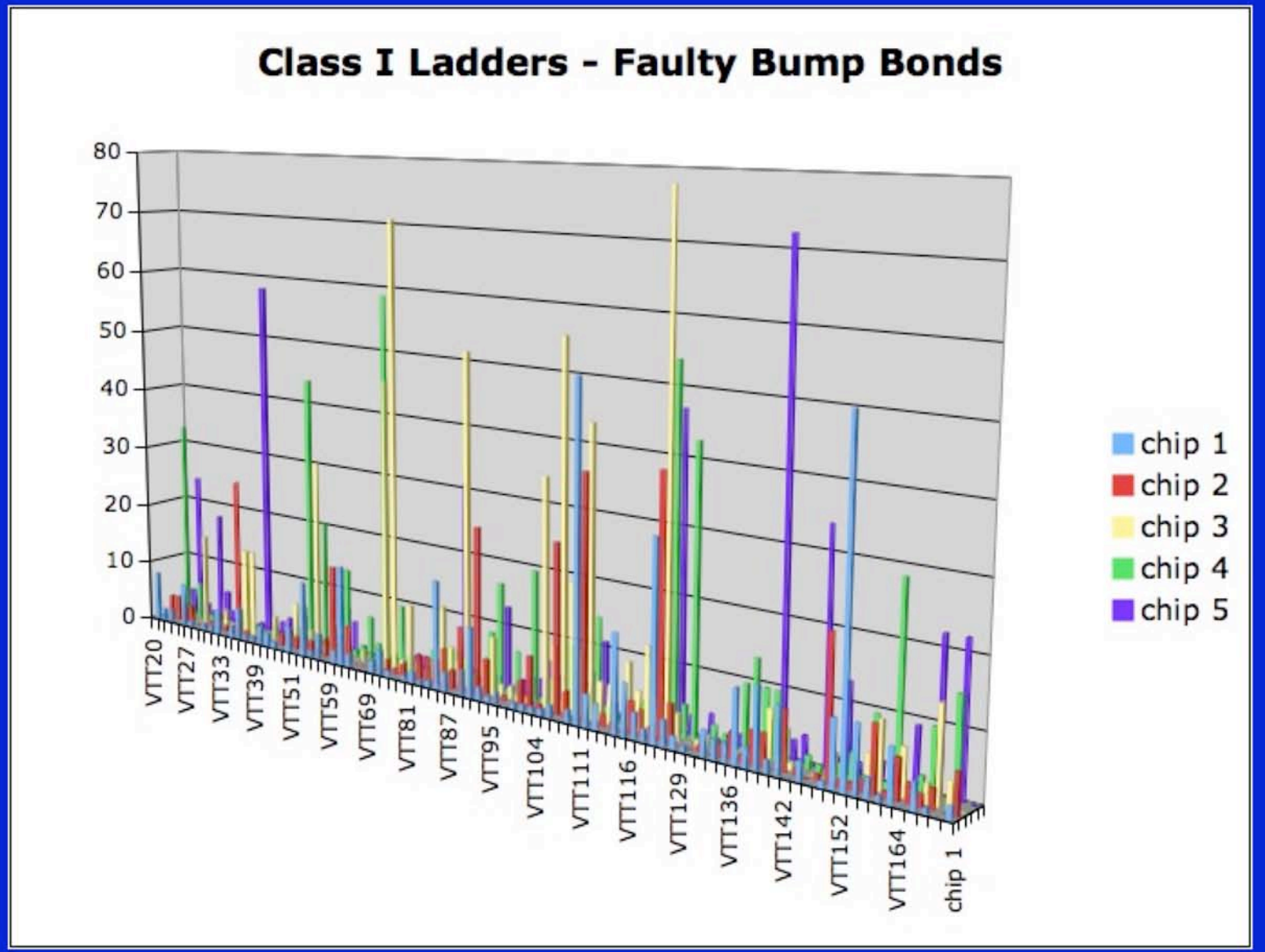
**5 readout chips/sensor**
**0.25$\mu$m CMOS**
**13.68 mm x 15.58 mm**

**p-in-n silicon sensor**
**72.72 mm x 13.92 mm**




**40960 bump bonds**
**~25 $\mu$m diameter**
**Stand-off:**
**~12 $\mu$m (Pb-Sn)**

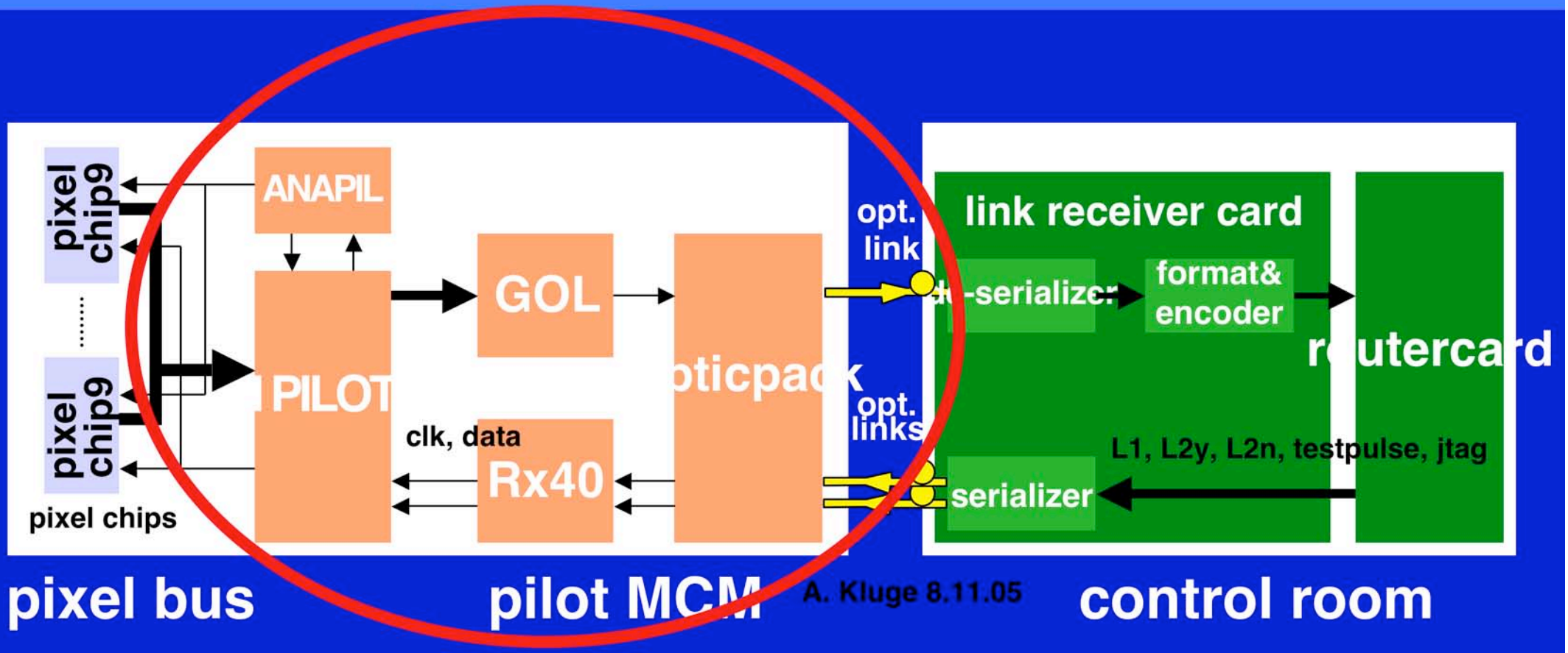
# Sensor & pixel chips



# On detector electronics elements

- The pixel chip & sensors
- **Multi chip module + ASICs**
- Al Multi-layer kapton cables (Bus)

# Pixel read out system



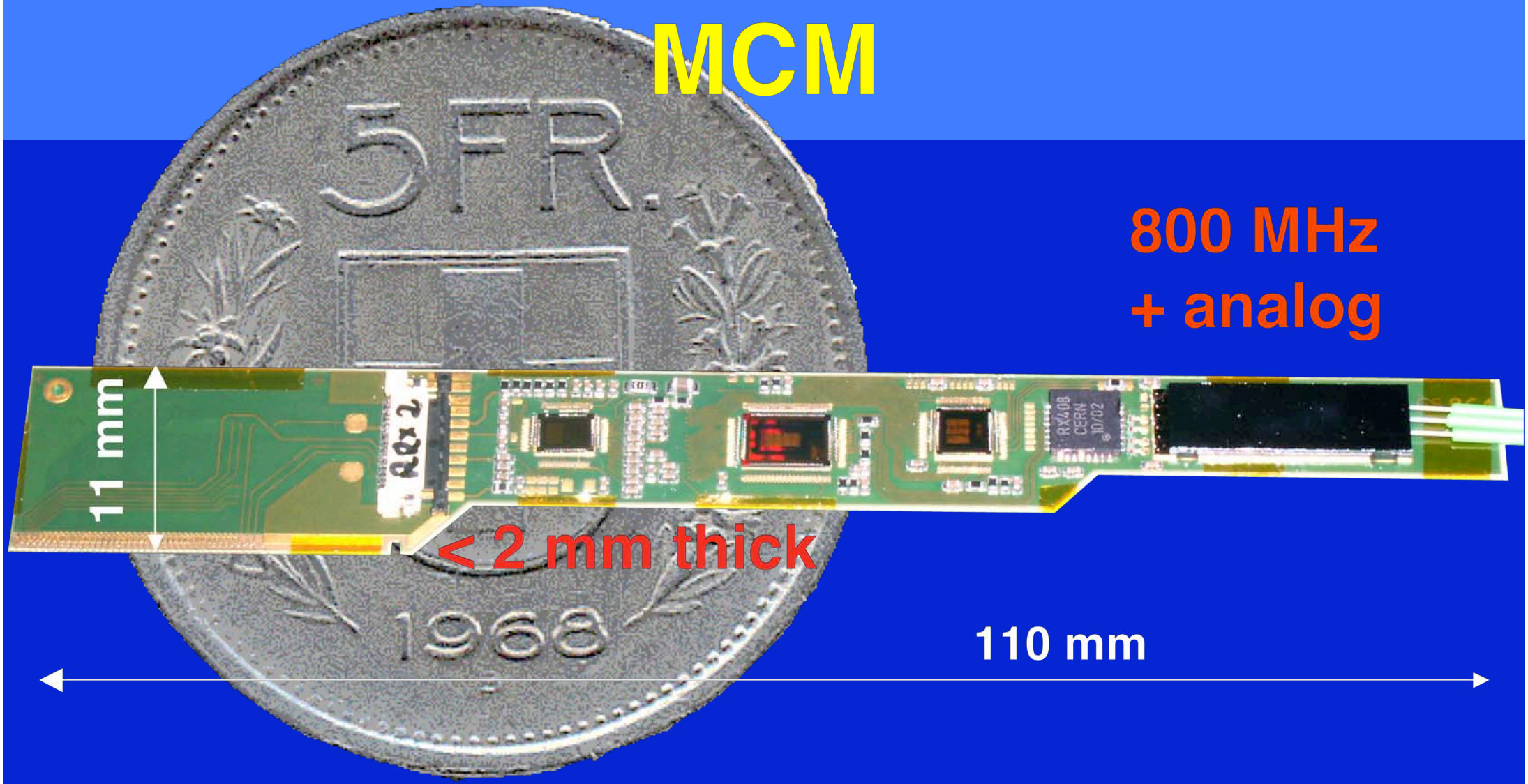
# MCM

800 MHz
+ analog


< 2 mm thick

110 mm

# MCM



# MCM

800 MHz
+ analog


< 2 mm thick

110 mm

# MCM

No Copper connections

No data processing, no memory

**800 MHz + analog**


**< 2 mm thick**

**110 mm**

Analog (10mV) + digital (800MHz)

Dense, comp. placement, routing

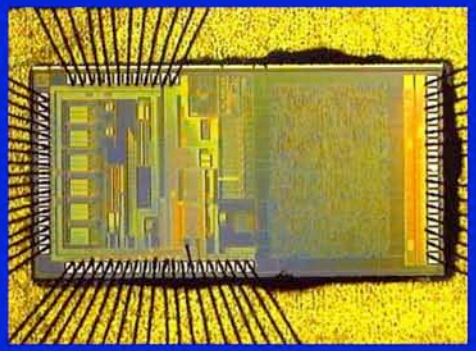
Fragile: thin, no packages

Small quantity

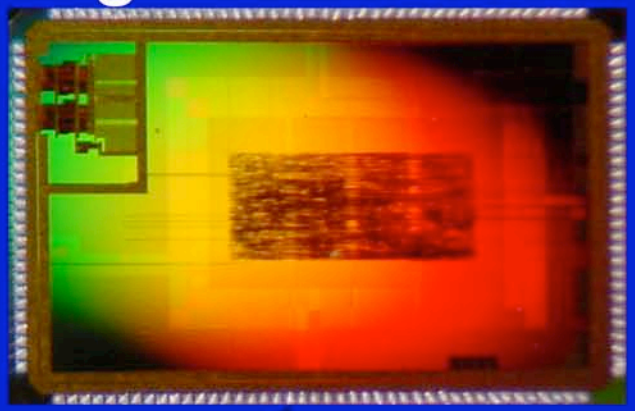
Small: no probing, limited reworking

# Pilot MCM ASICs

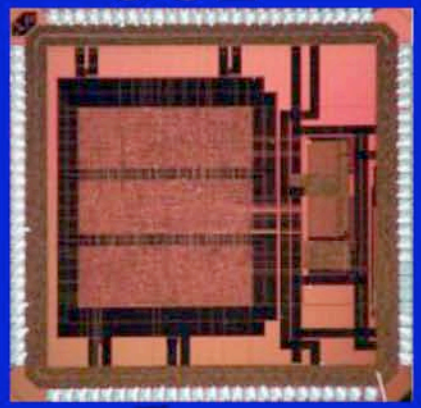
ANAPIL3



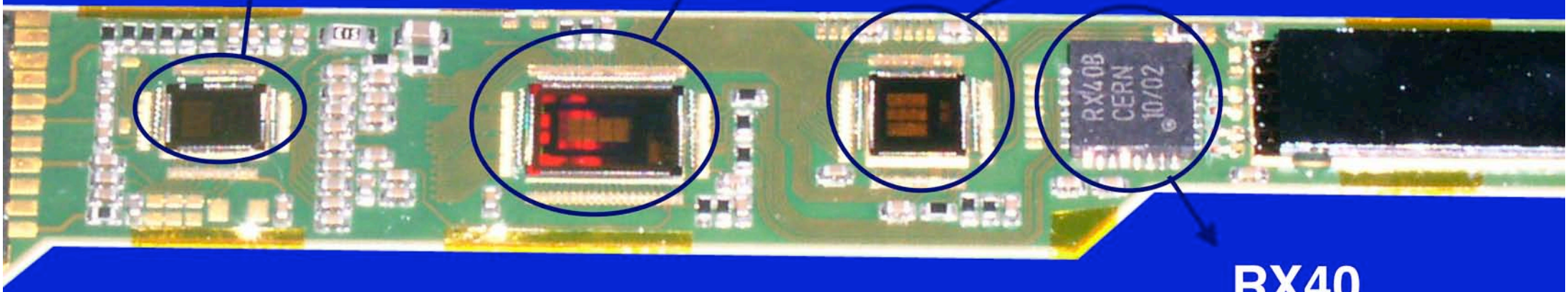
Digital Pilot 2003



GOL

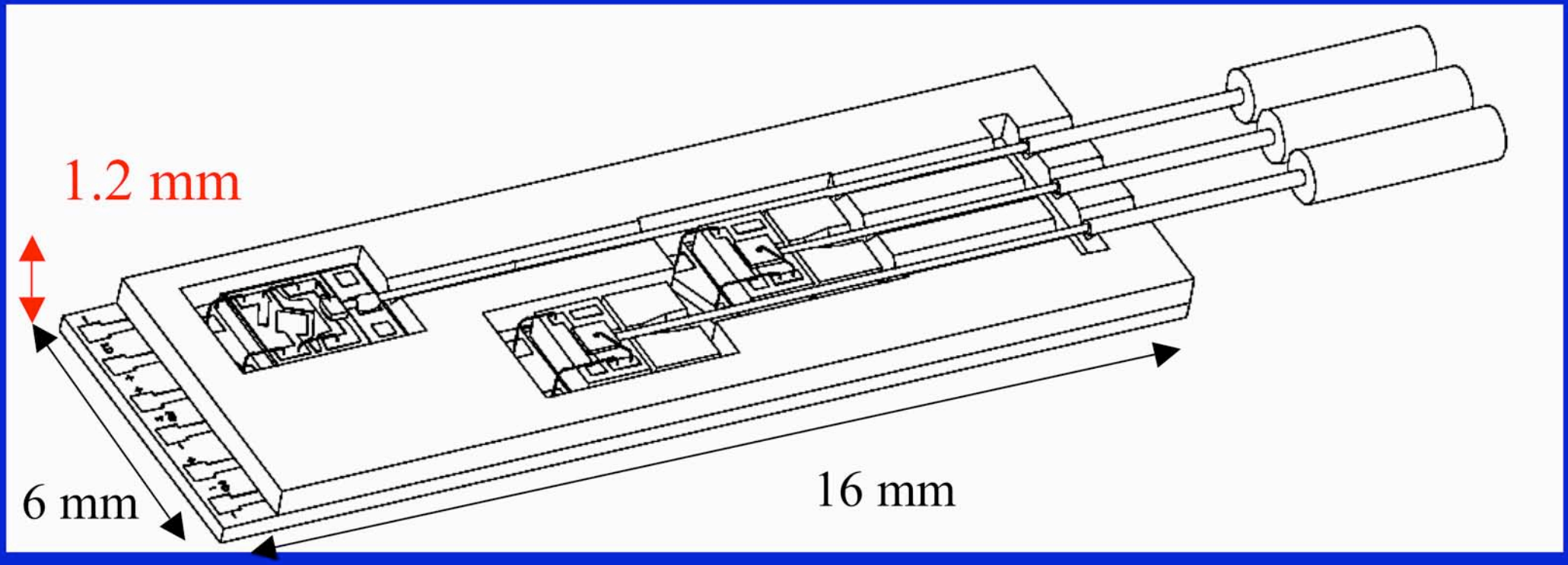


PILOT MCM



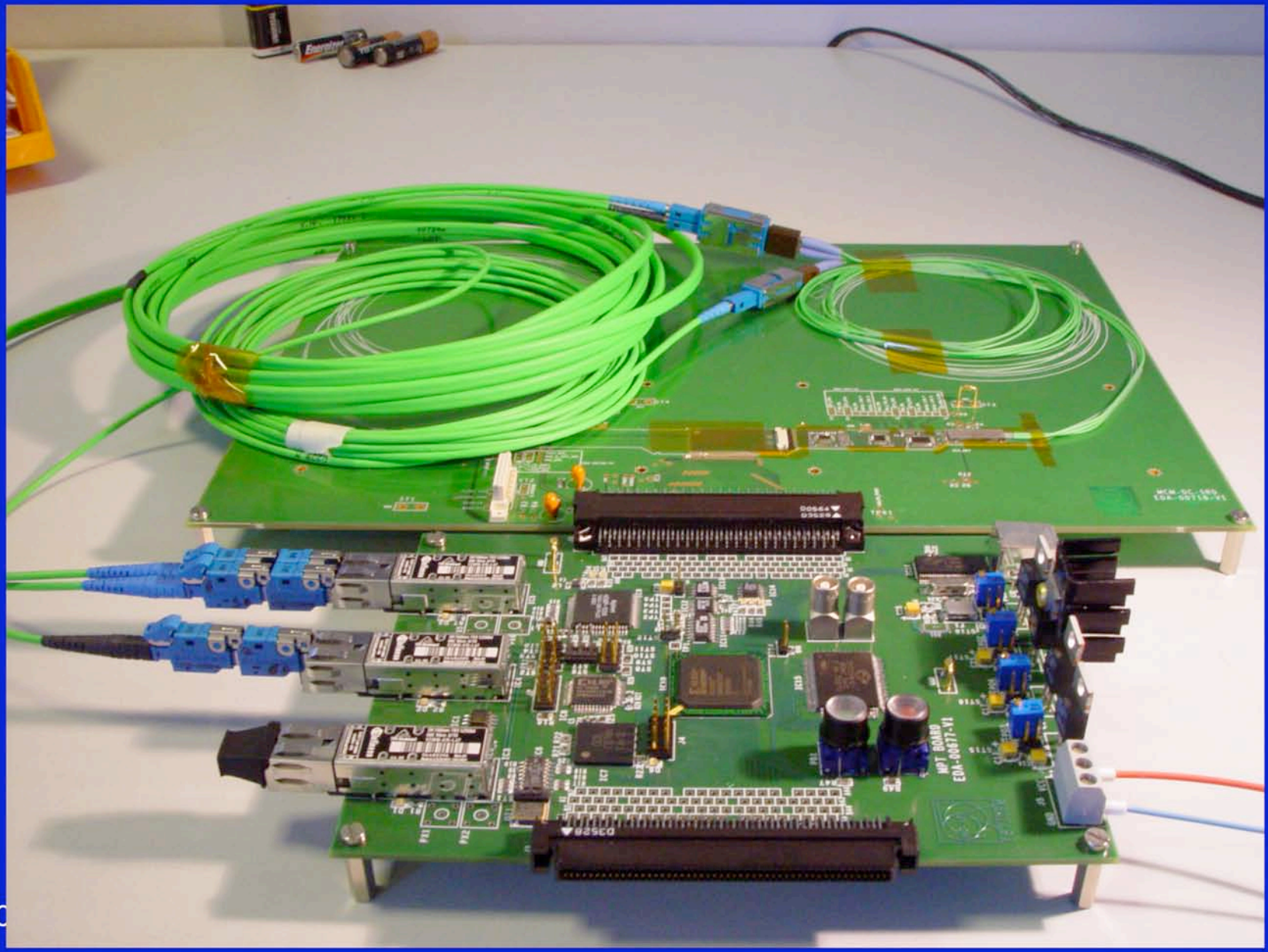

RX40

# Pilot MCM Optical package

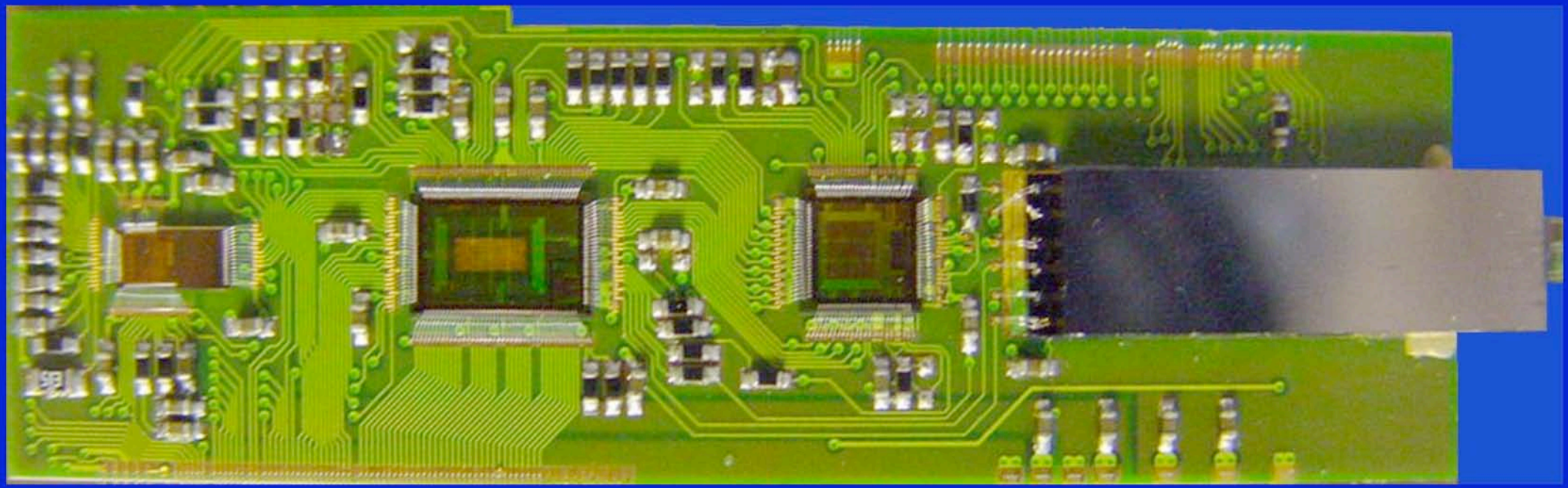



link has 15 dB input and output optical margin

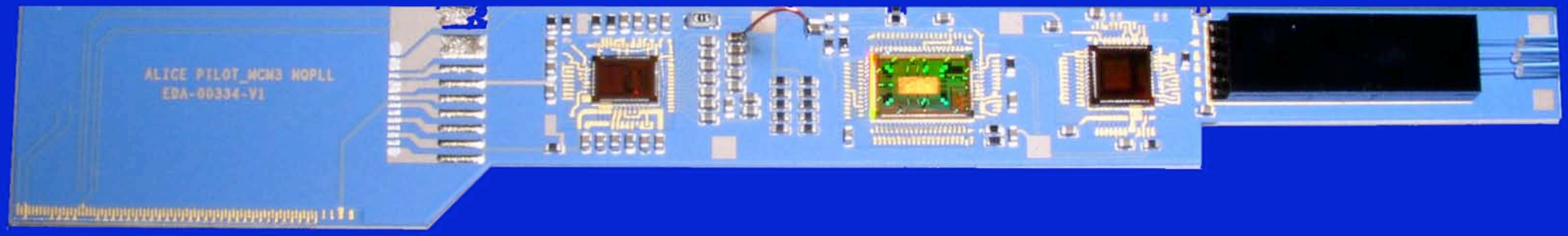
# MCM



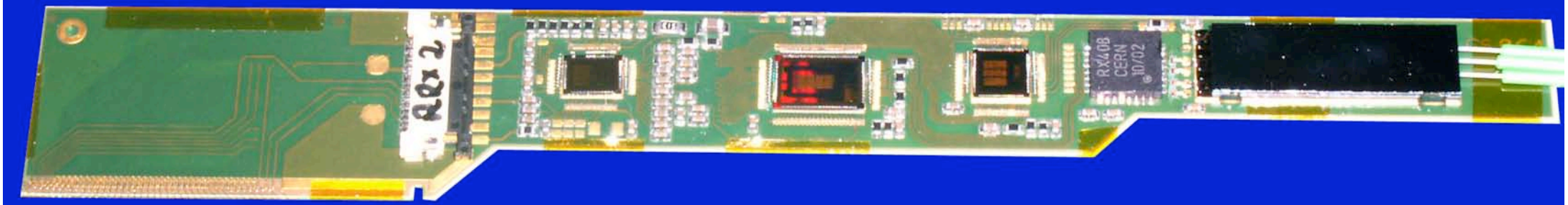
# Pilot MCM ASICs



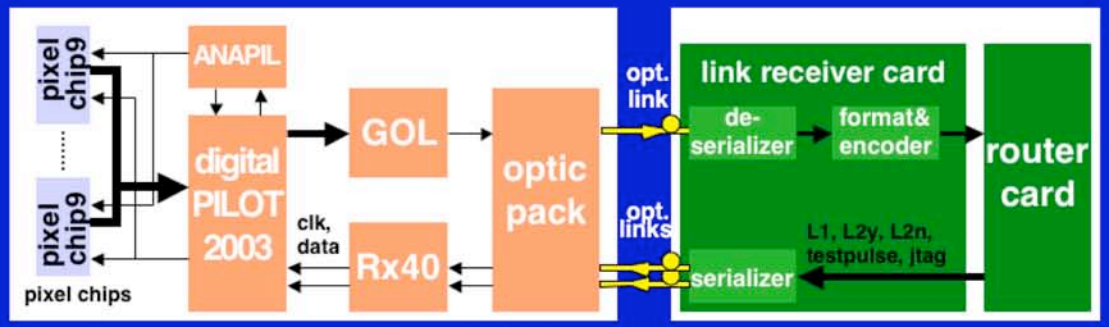
# Pilot MCM ASICs



# MCM



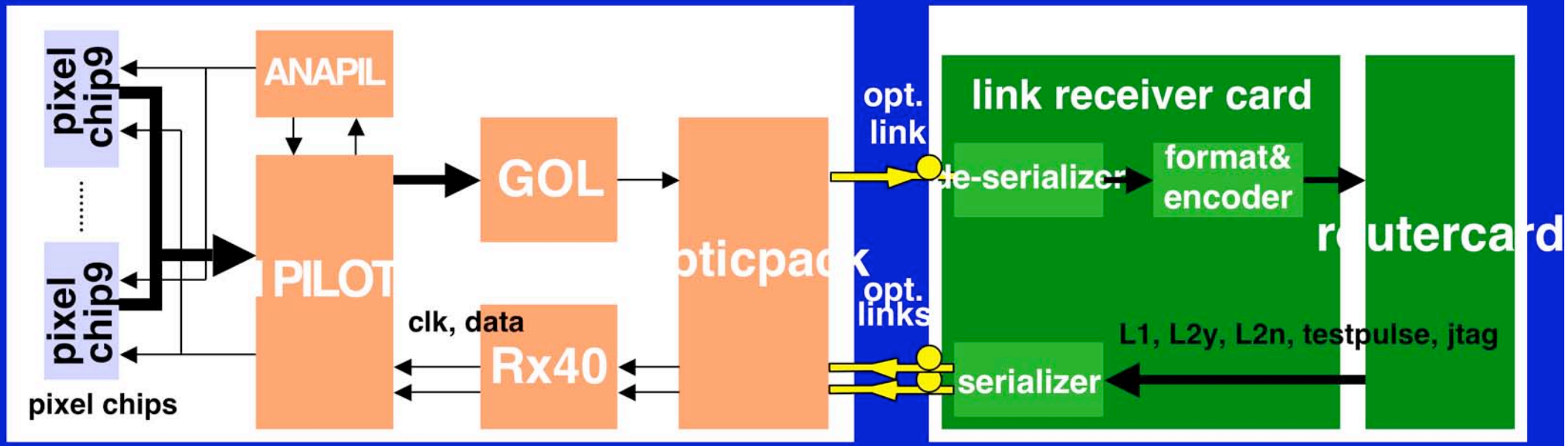

Complexity due to connectivity, limited space, number of signals (bus width, analog bias) and late integration design.



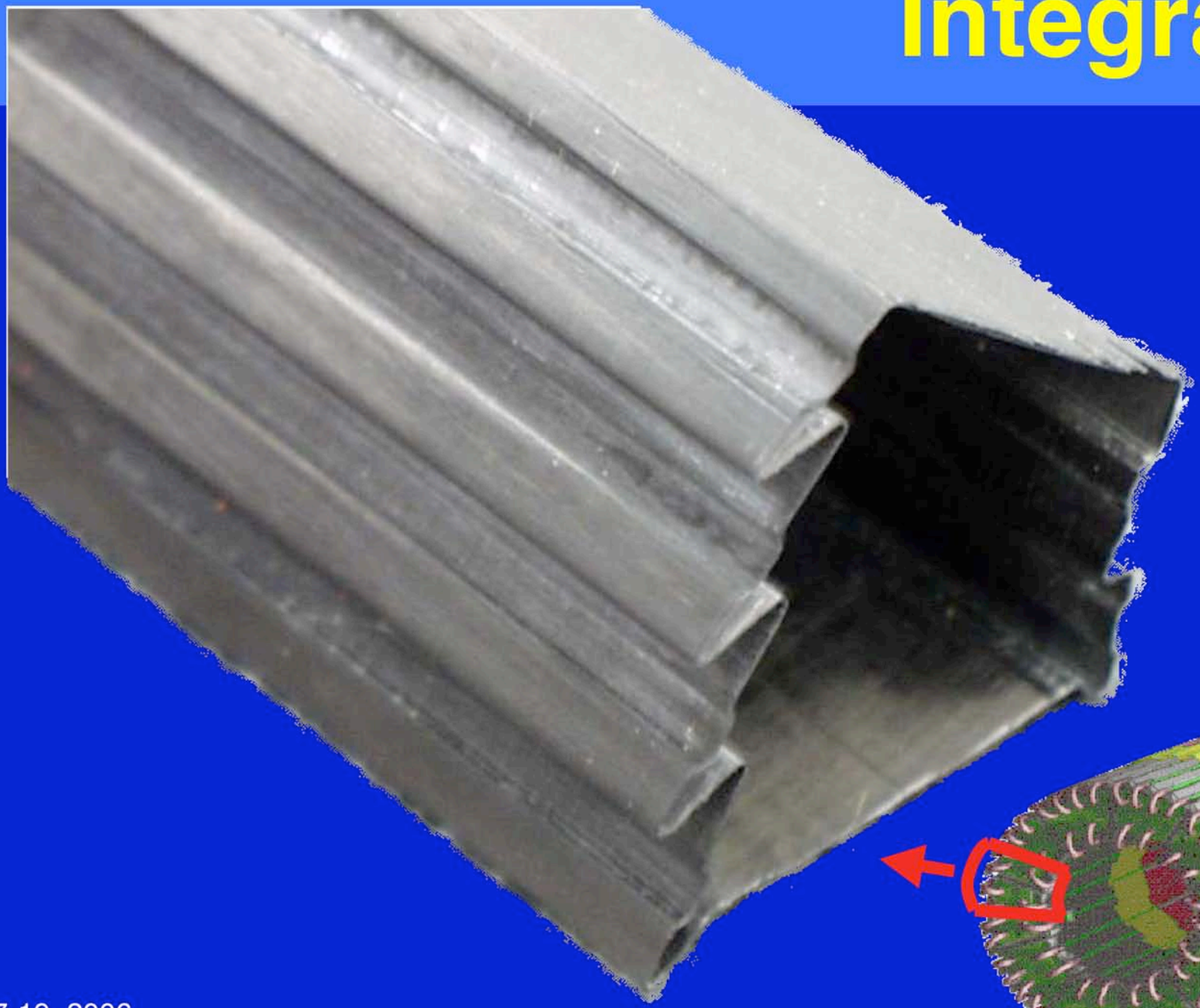
# On detector electronics elements

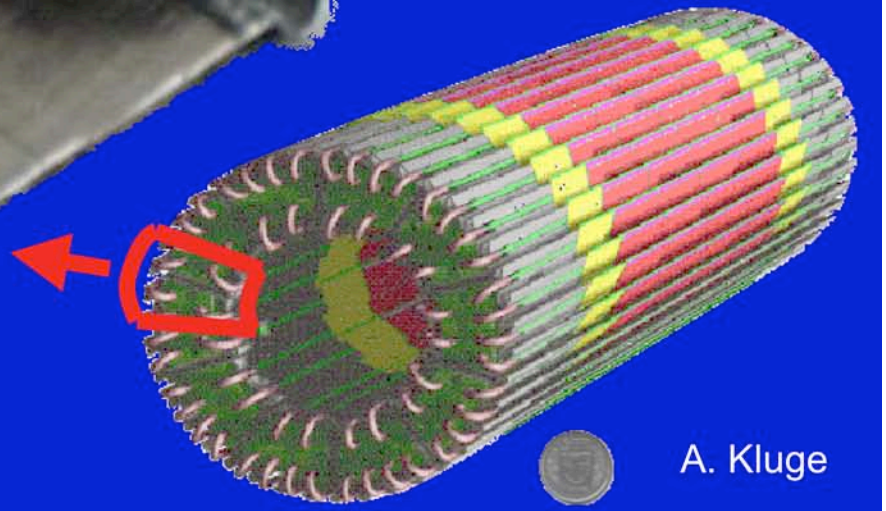
- The pixel chip & sensors
- Multi chip module + ASICs
- Al Multi-layer kapton cable (Bus)

# Pixel read out system

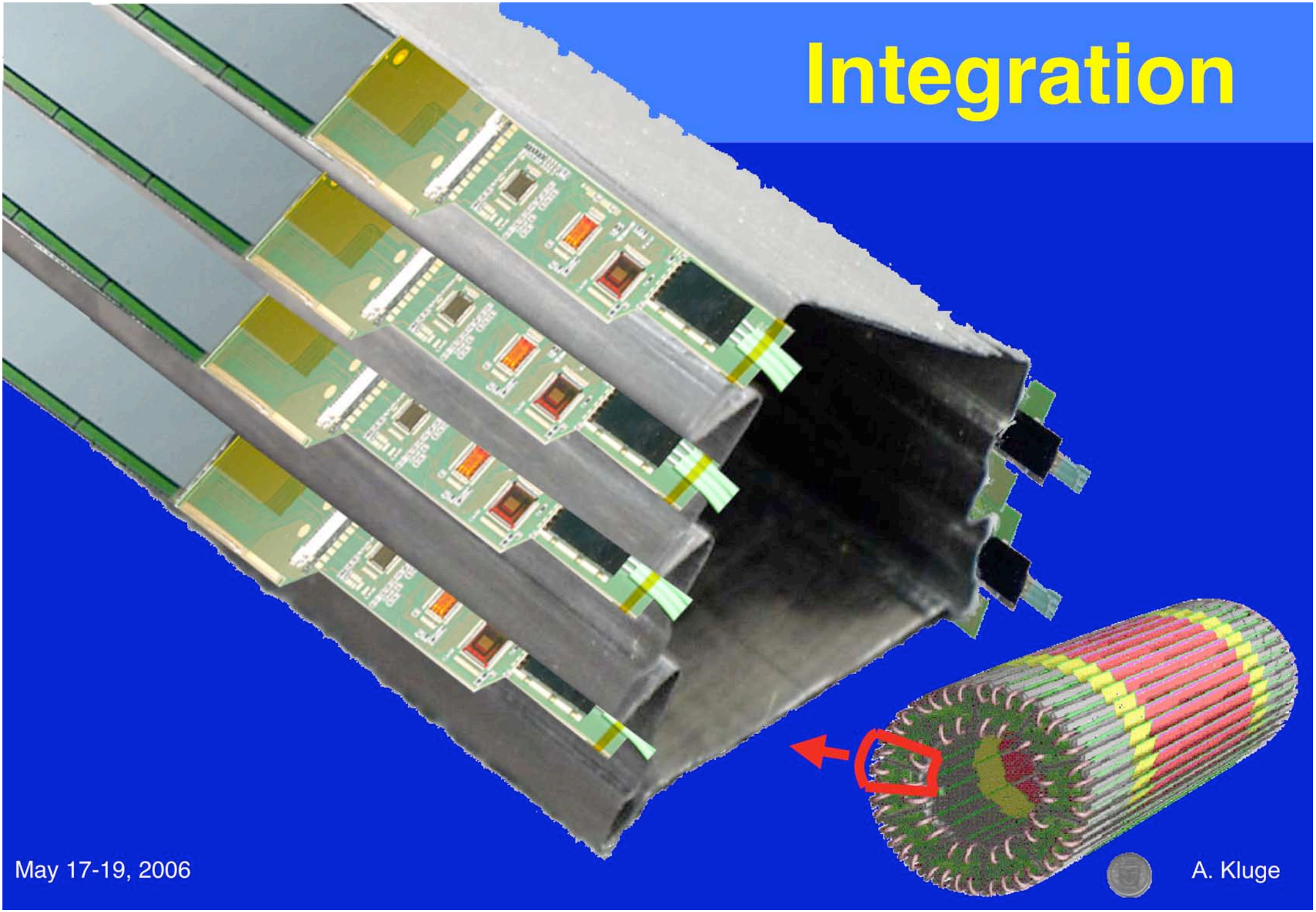


# Integration

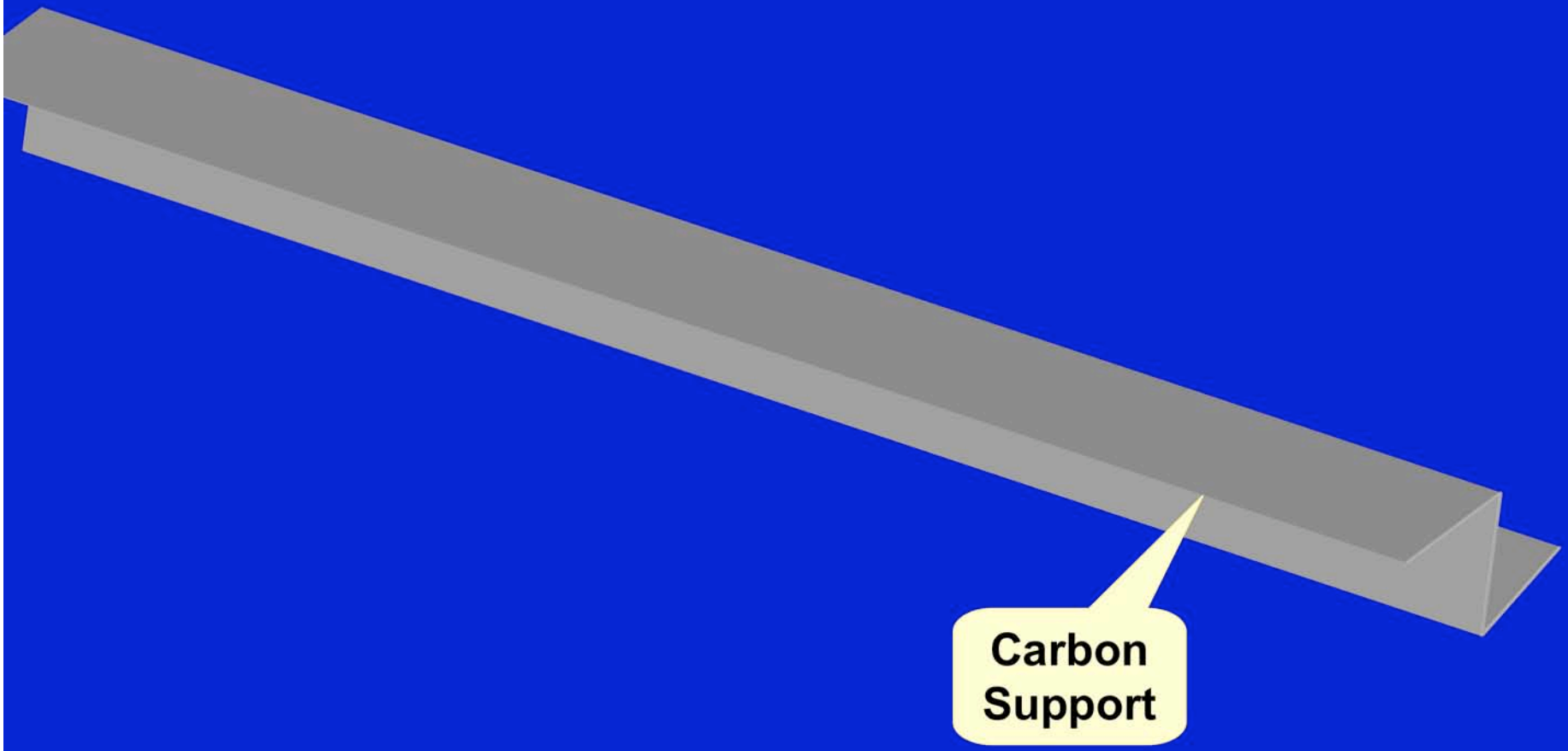




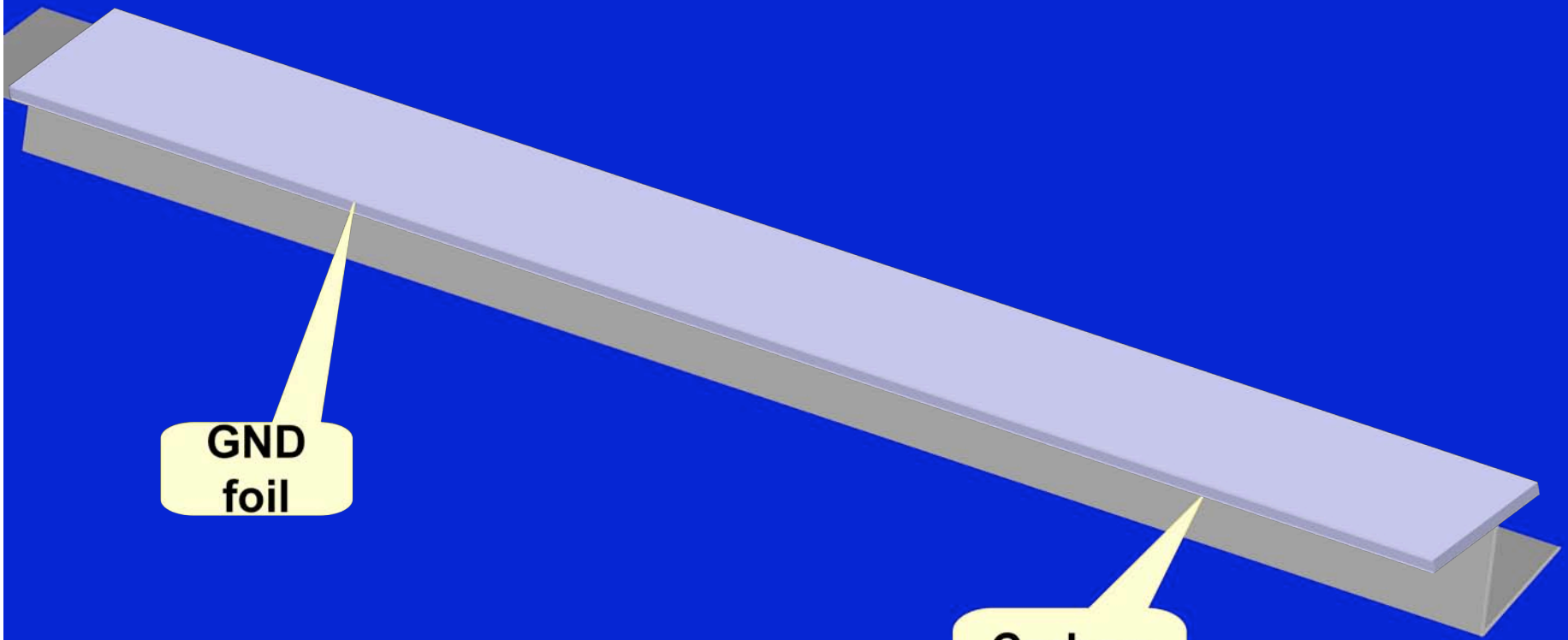
# Integration



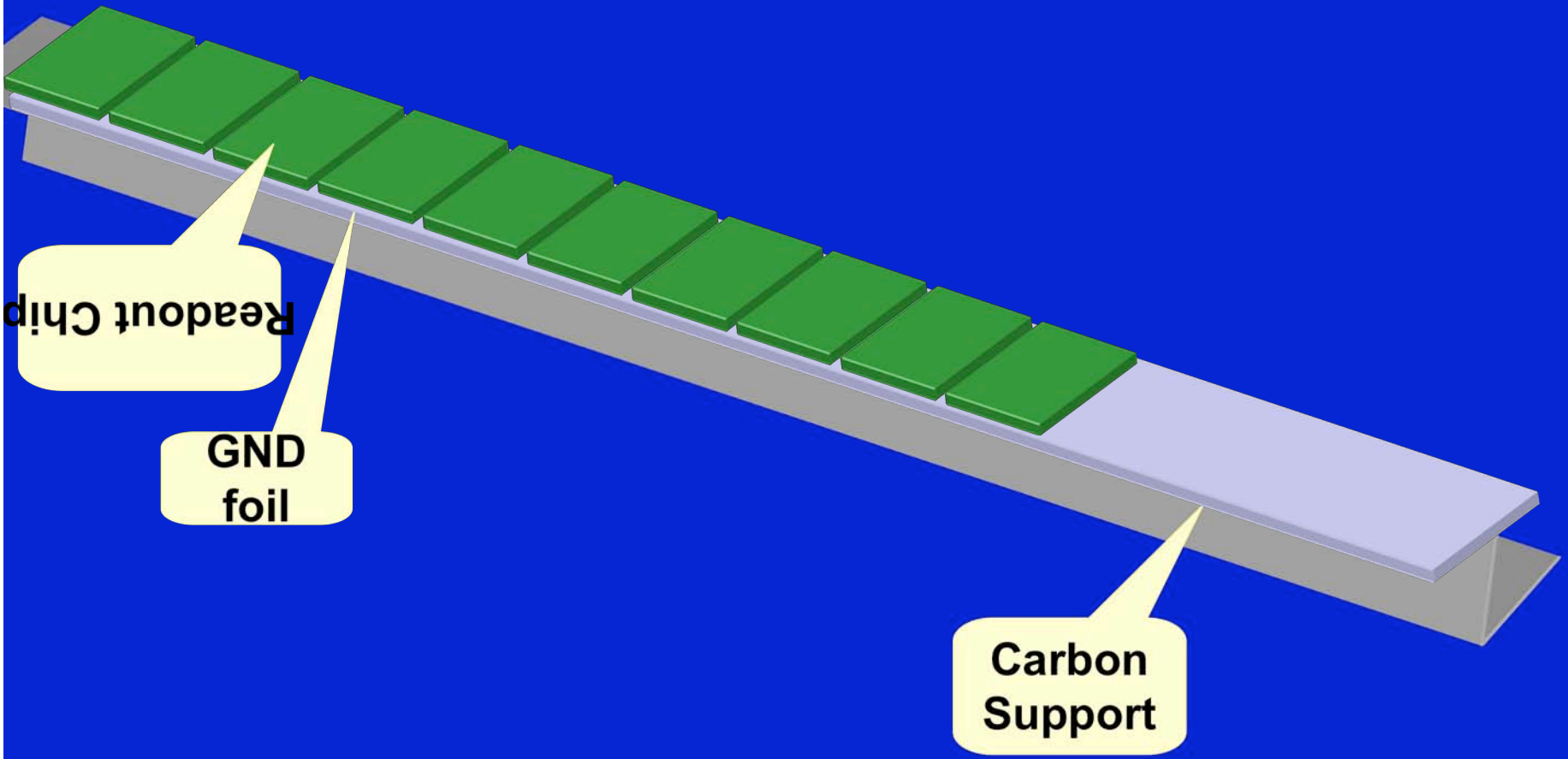
# Electronics integration



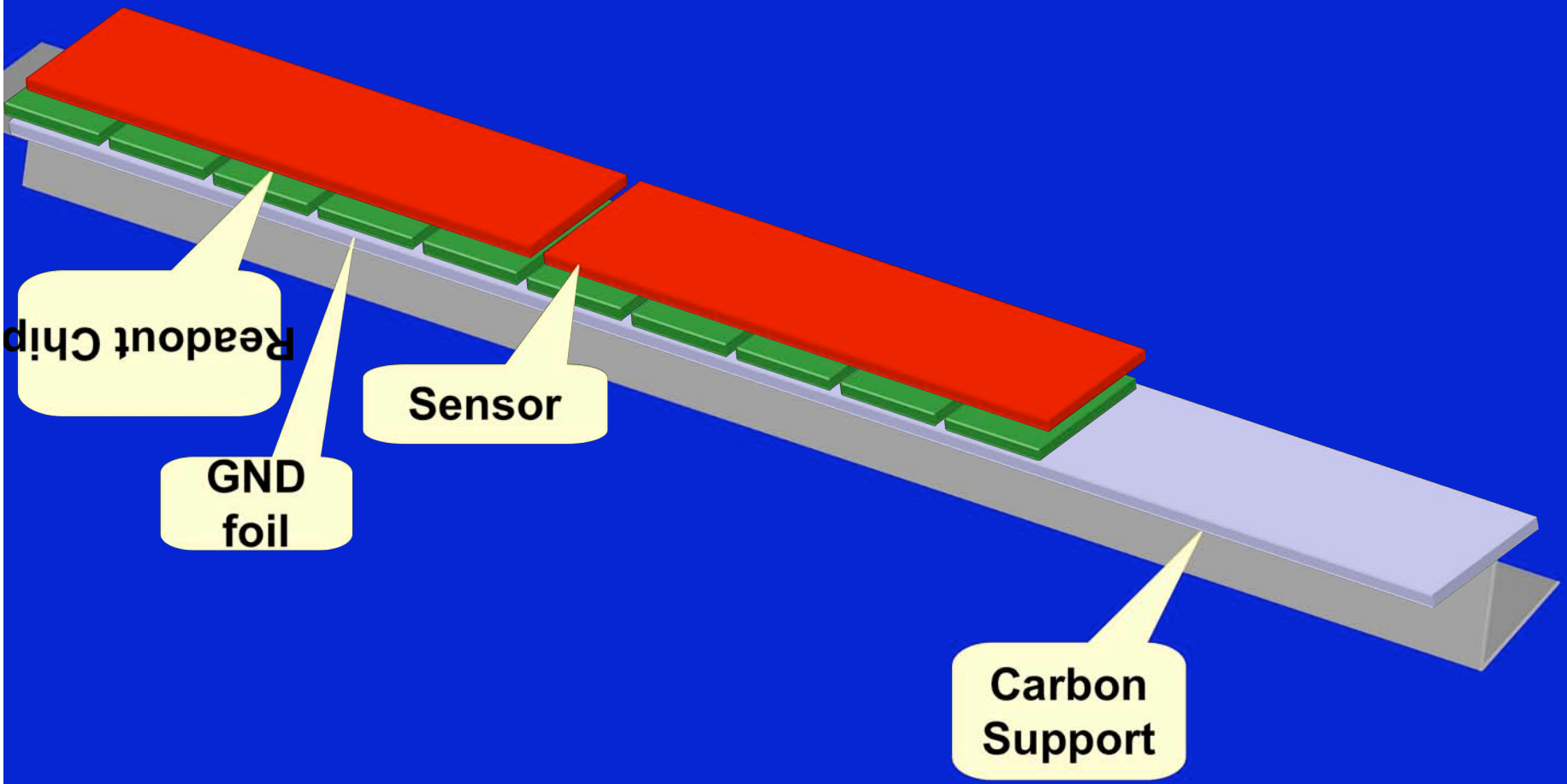
# Electronics integration



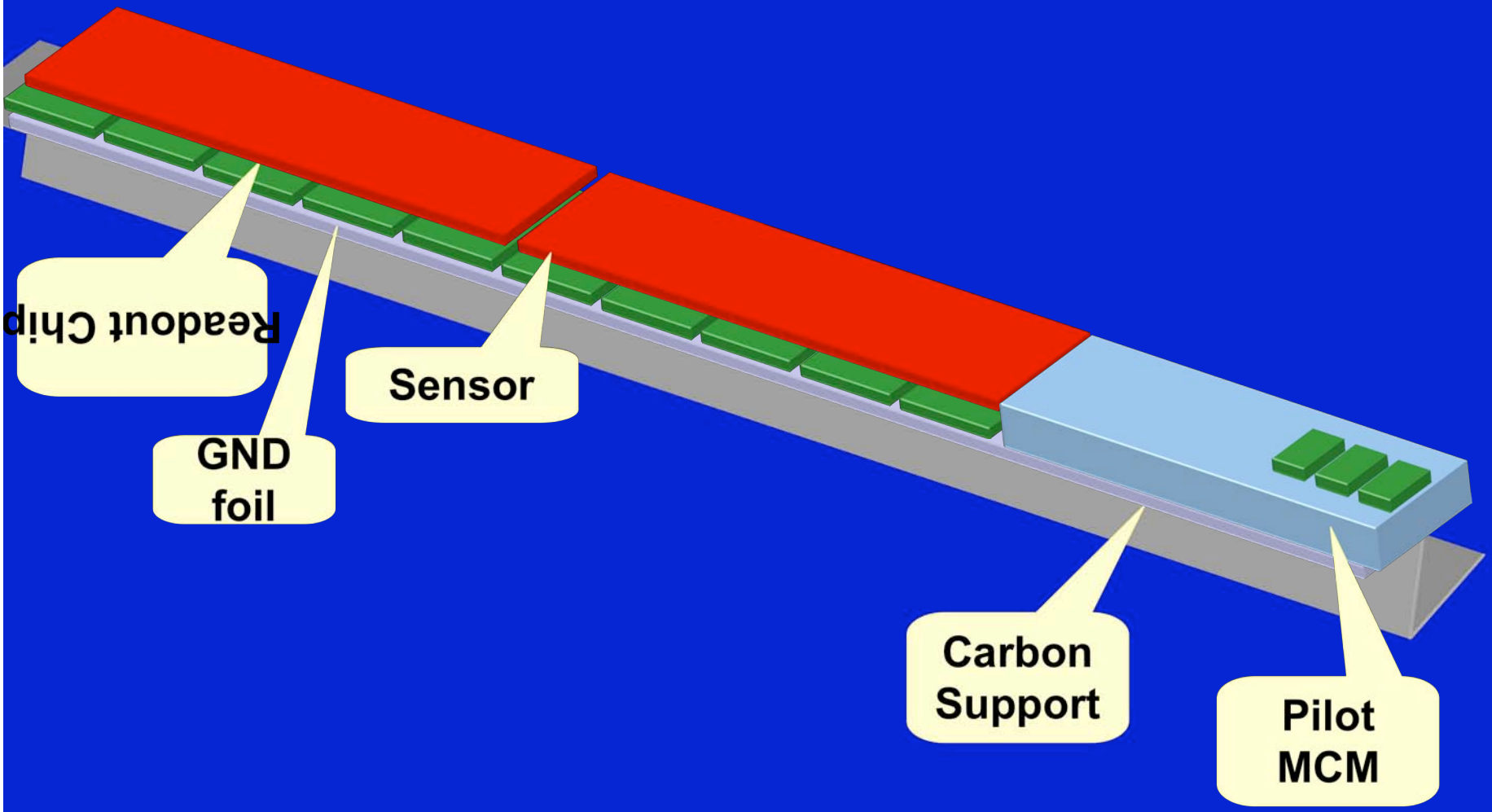
# Electronics integration



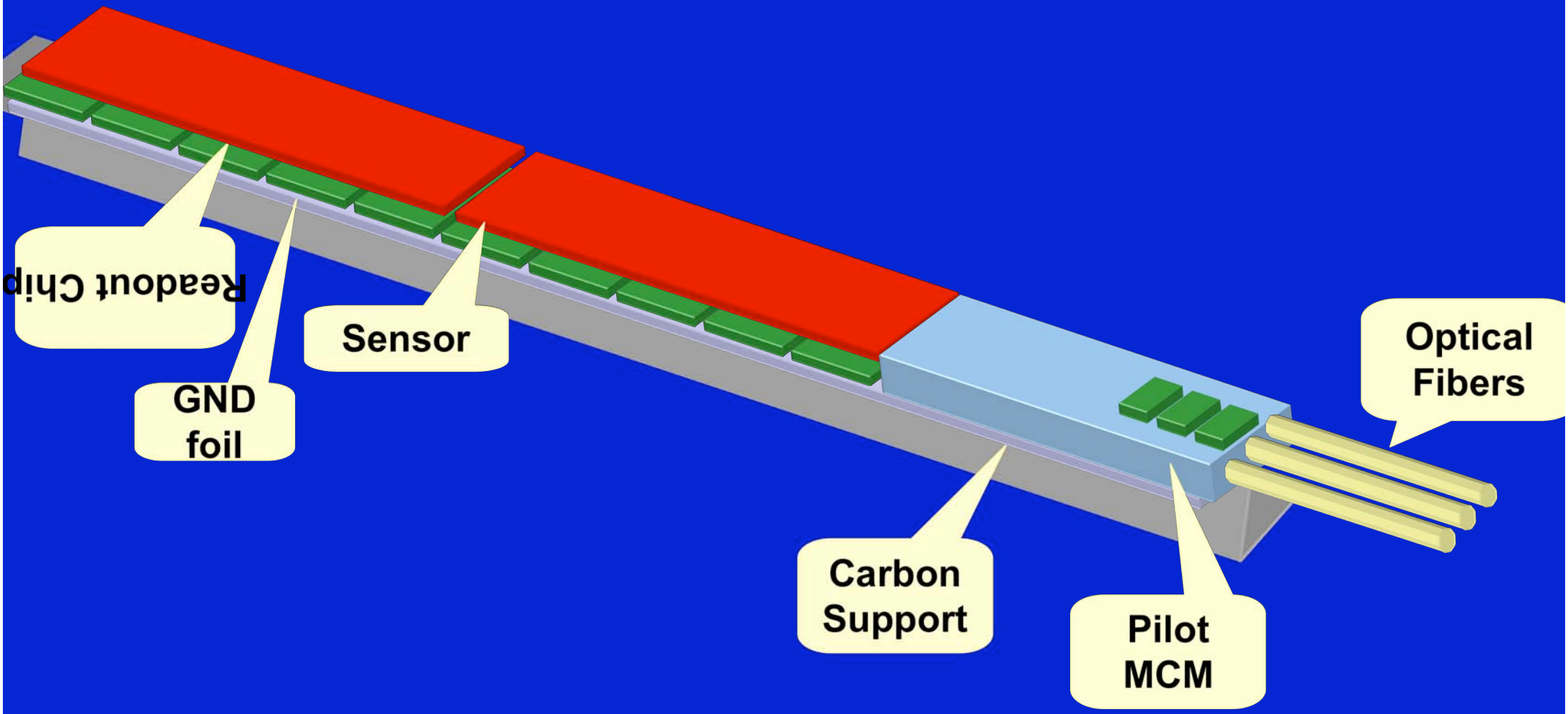
# Electronics integration



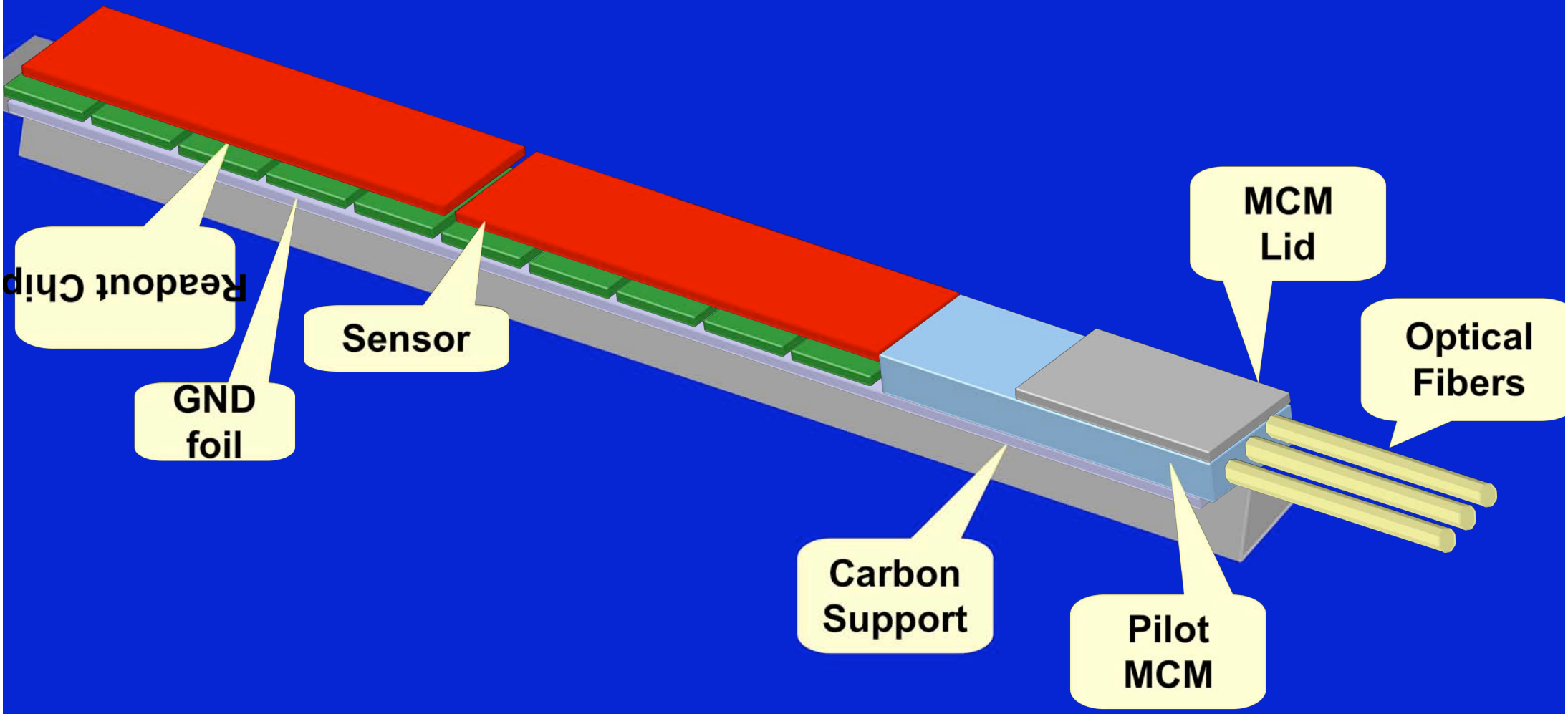
# Electronics integration



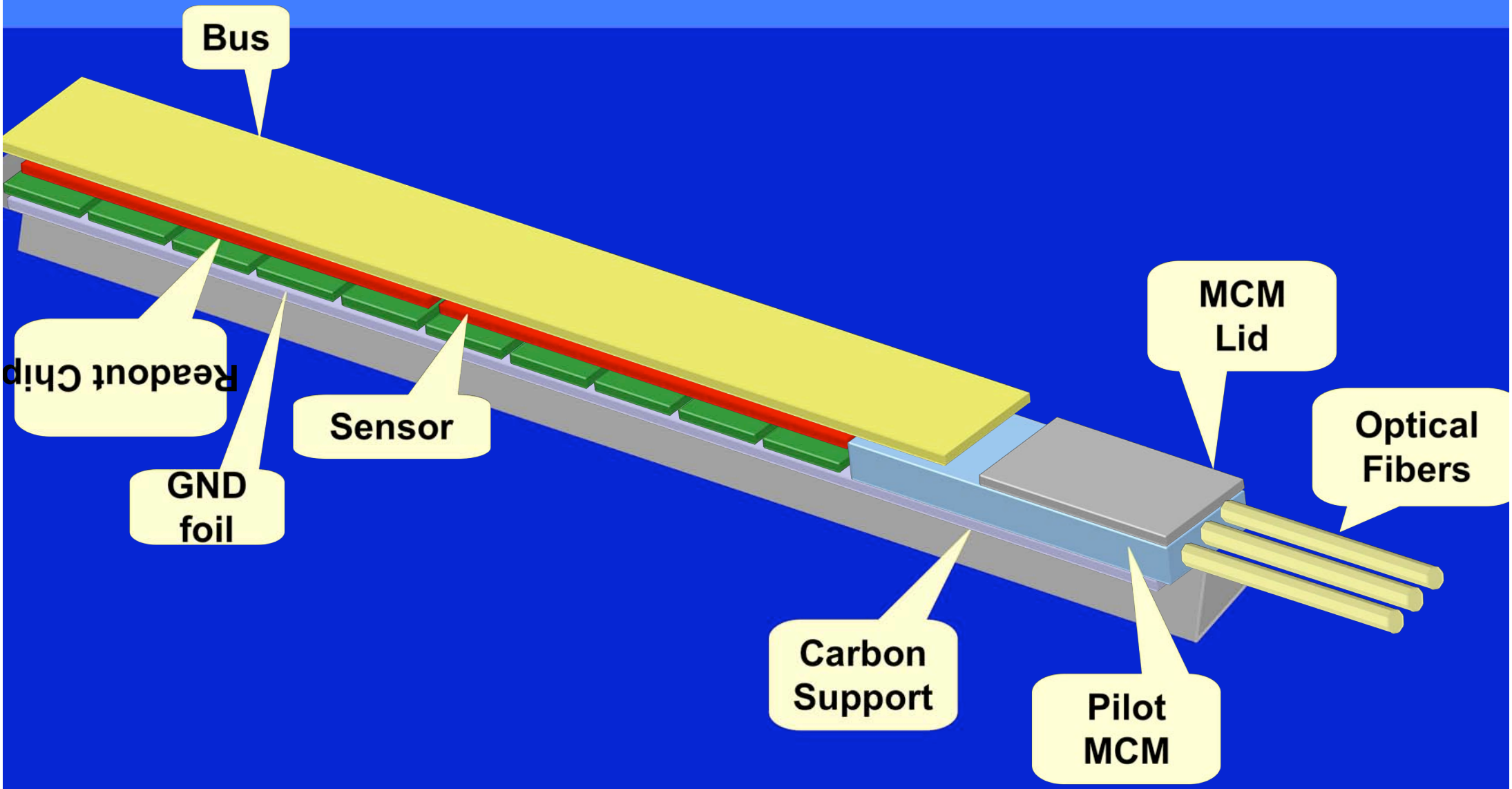
# Electronics integration



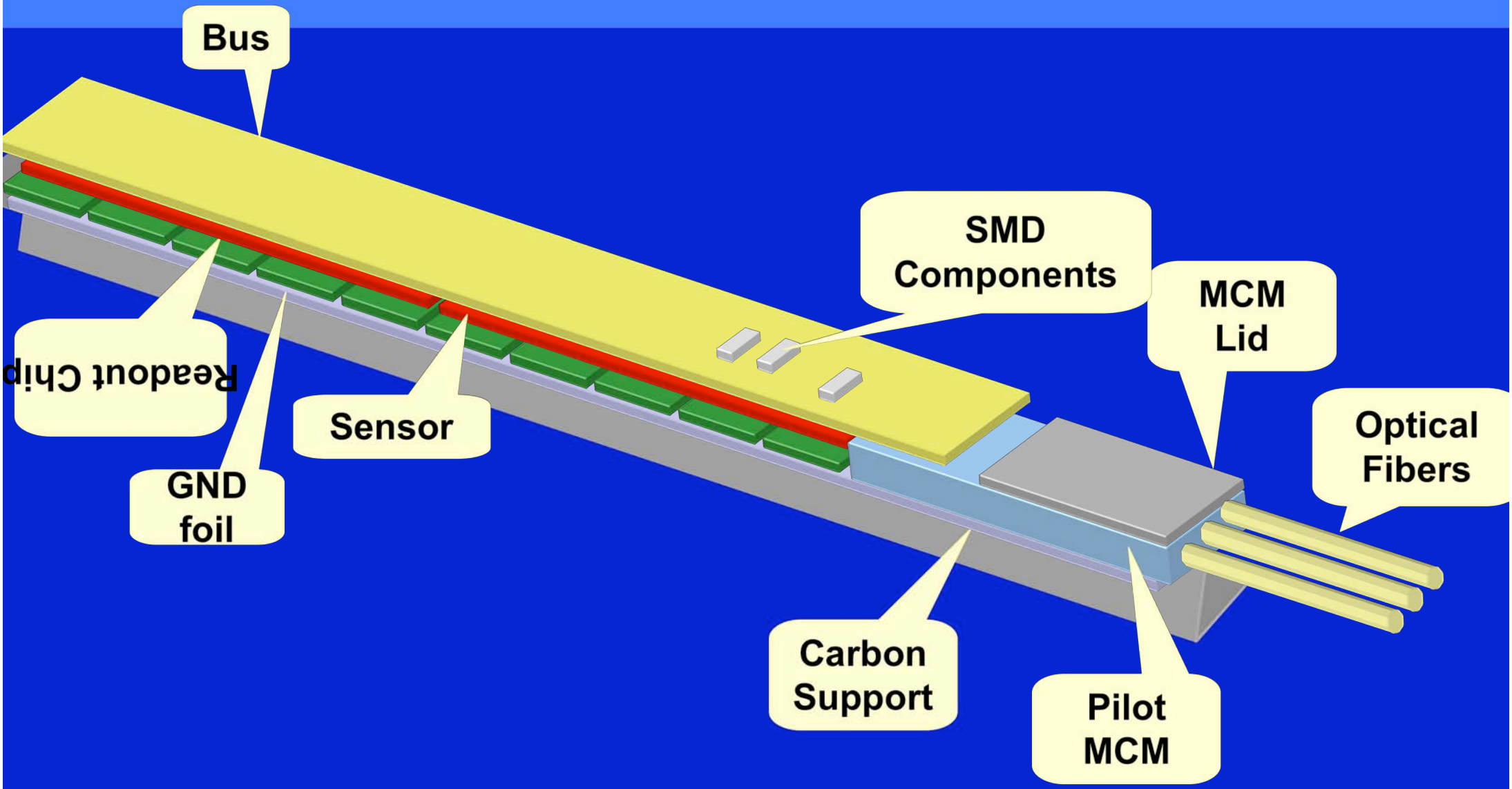
# Electronics integration



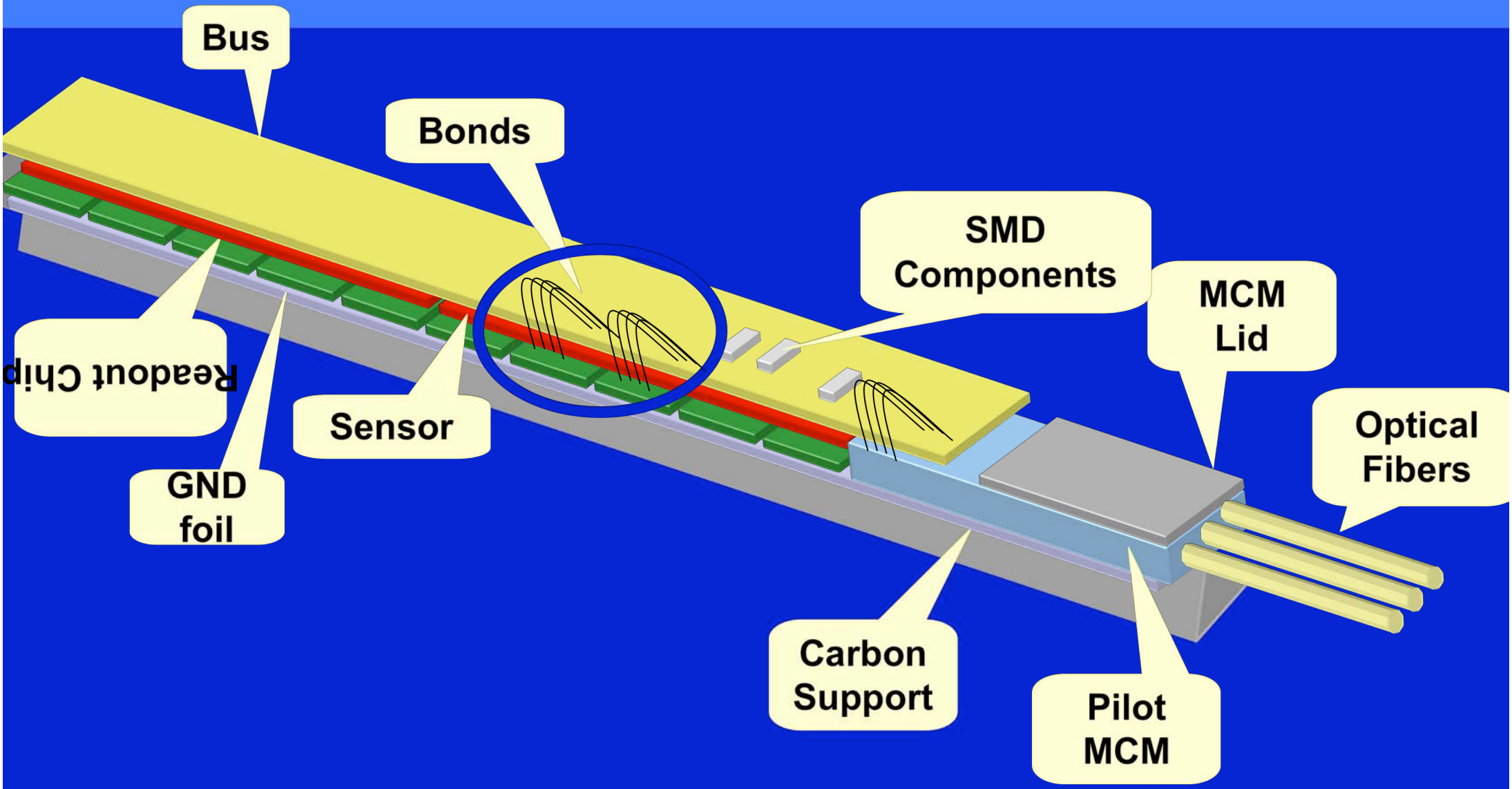
# Electronics integration



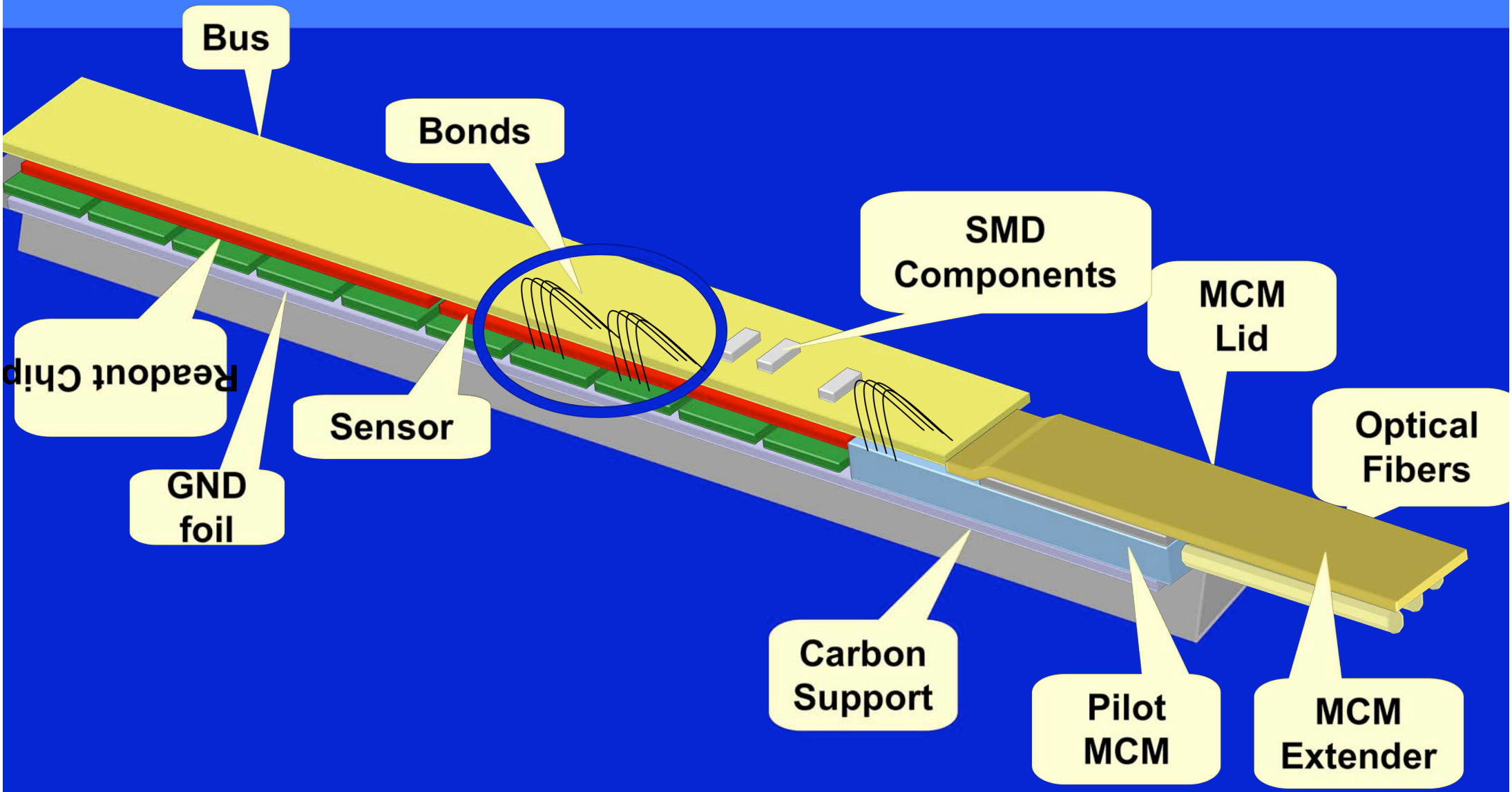
# Electronics integration



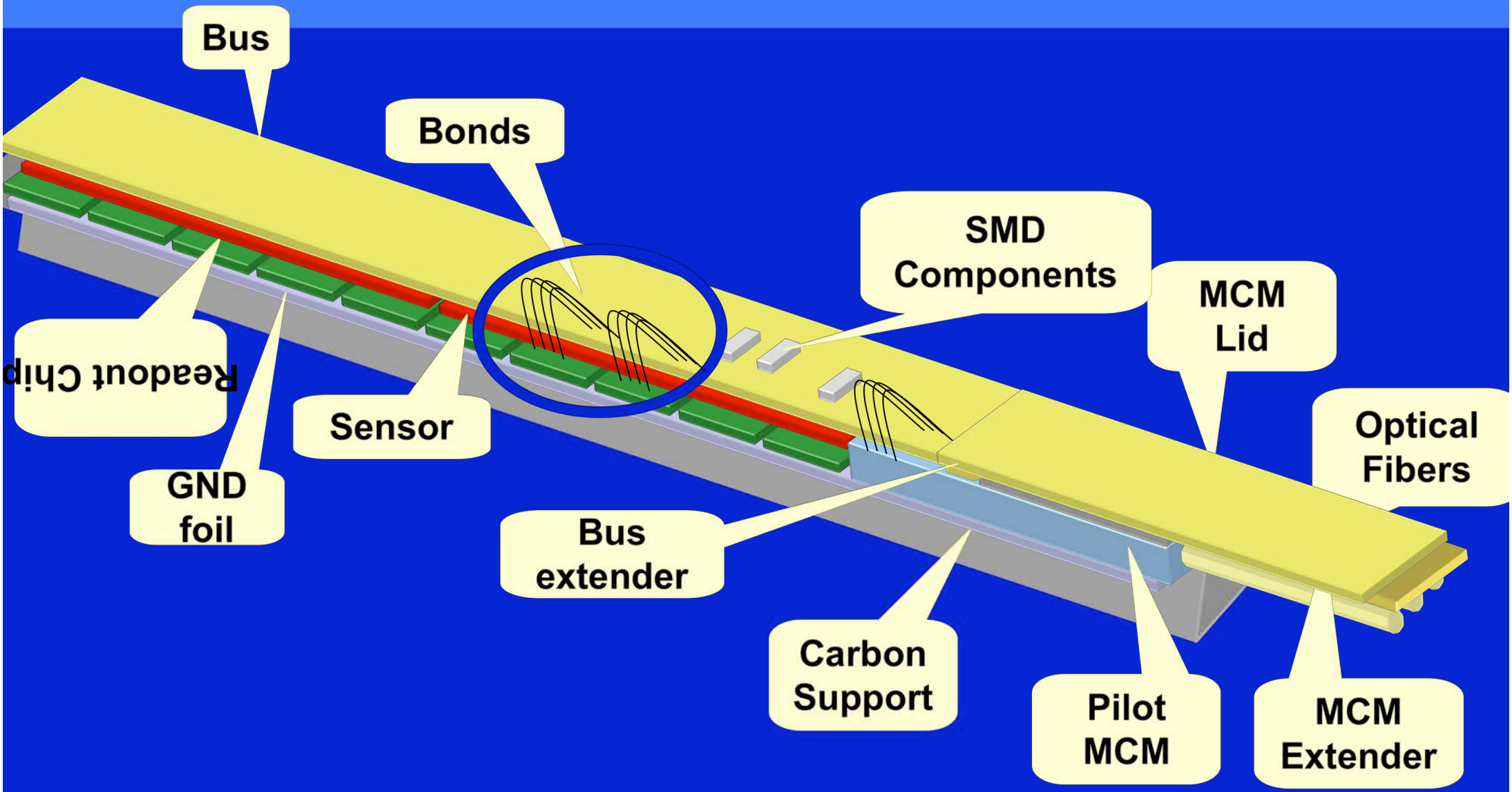
# Electronics integration



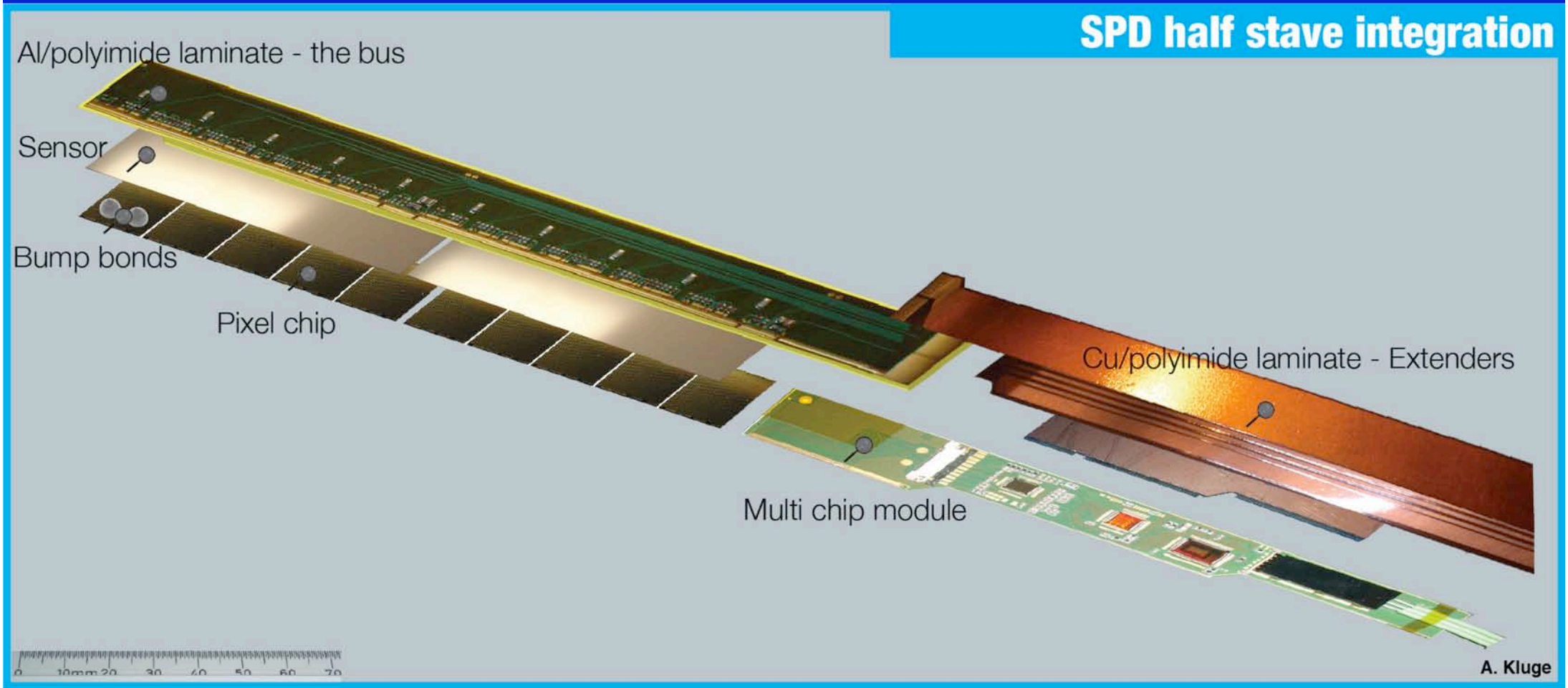
# Electronics integration



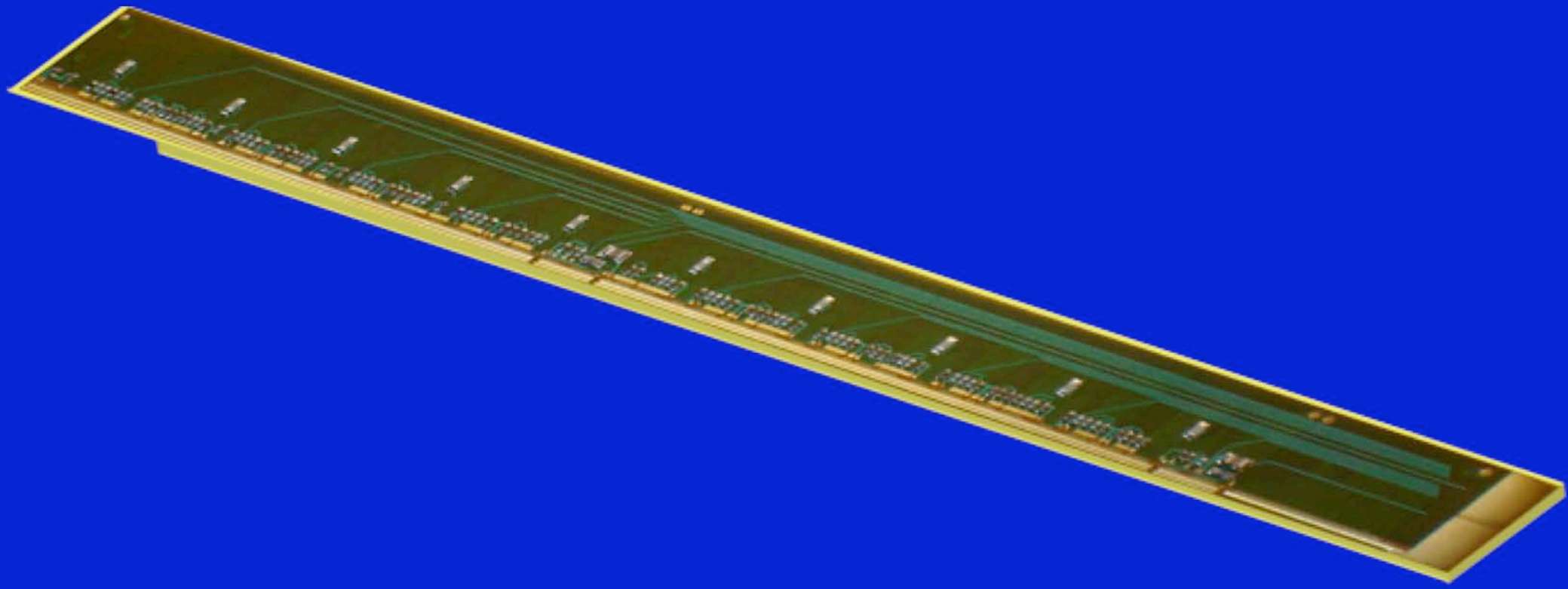
# Electronics integration



# Electronics integration



# The pixel bus



# The pixel bus

- Aluminum
- Length: ~ 20 cm, width ~13 mm
- Total thickness: 220 μm
- 5 layers: Power, GND, 3 signal layers
- Each layer thickness: 10 μm to 50 μm
- Distance of bonding pads: 150 μm

# The pixel bus

Material budget -> Aluminum, thin

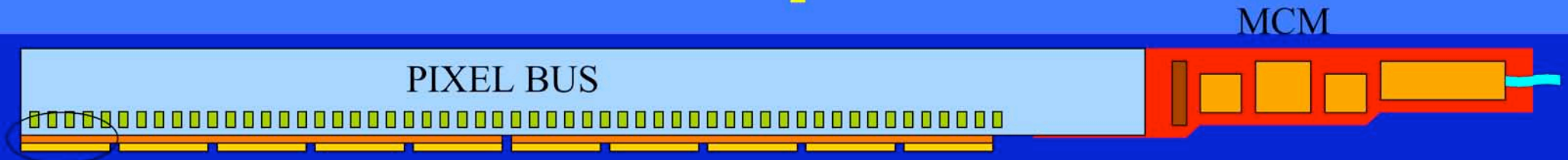
No industrial solution -> industry not interested

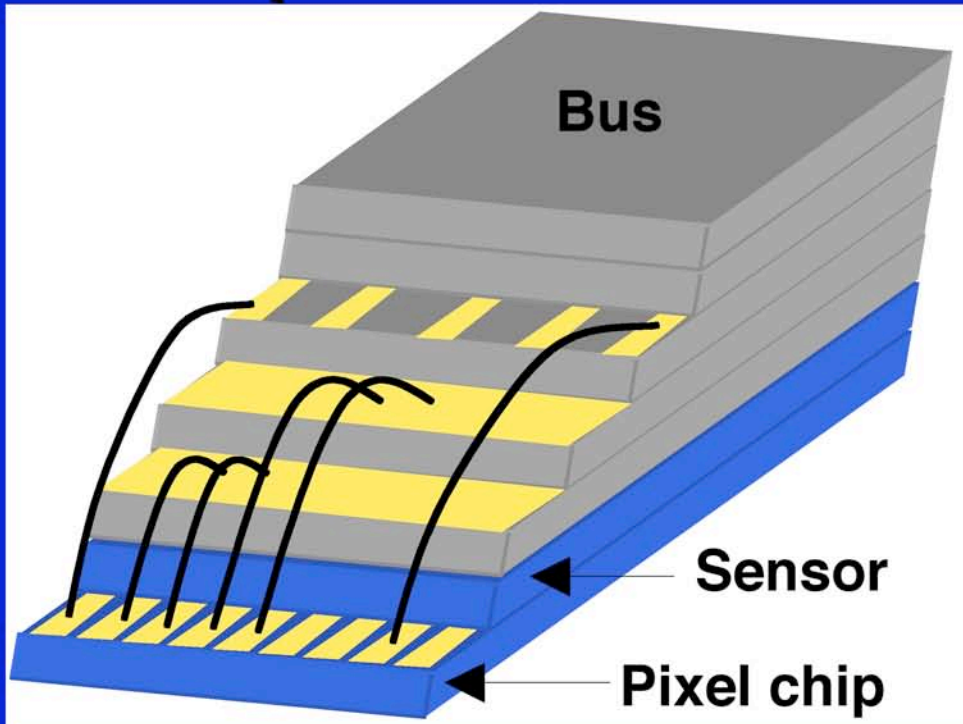
No previous experience in industry or research of Aluminium thin multi layer structures

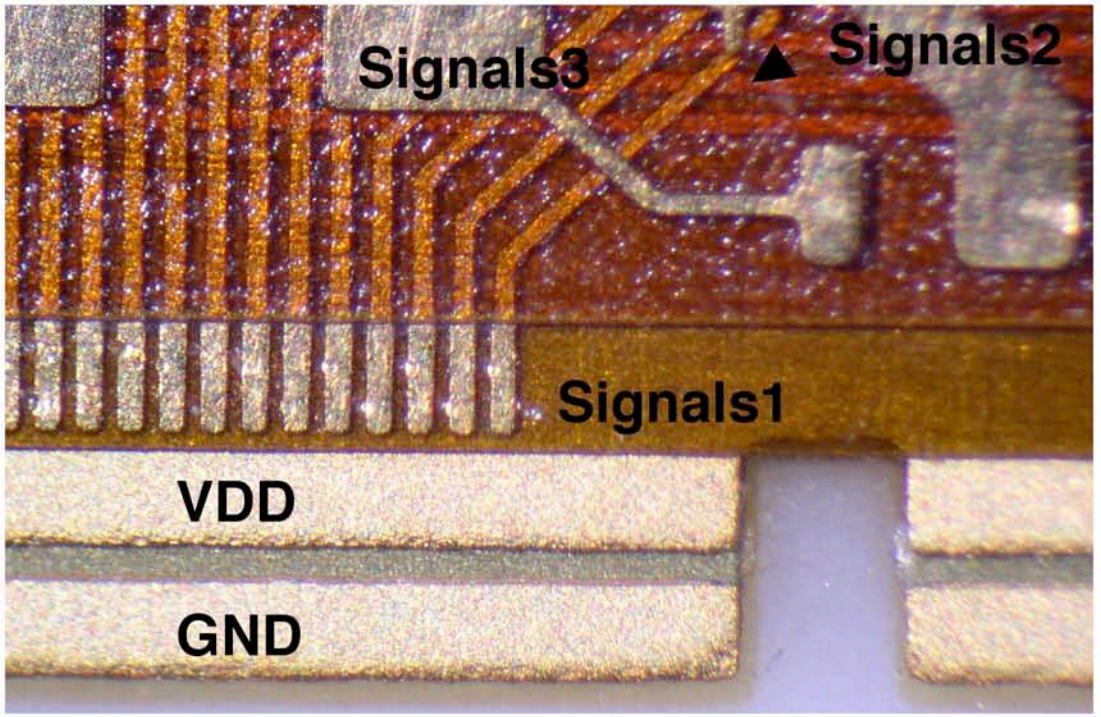
Connections between layers (vias) are difficult to make

Vias only for signals
Power uses stair case structure

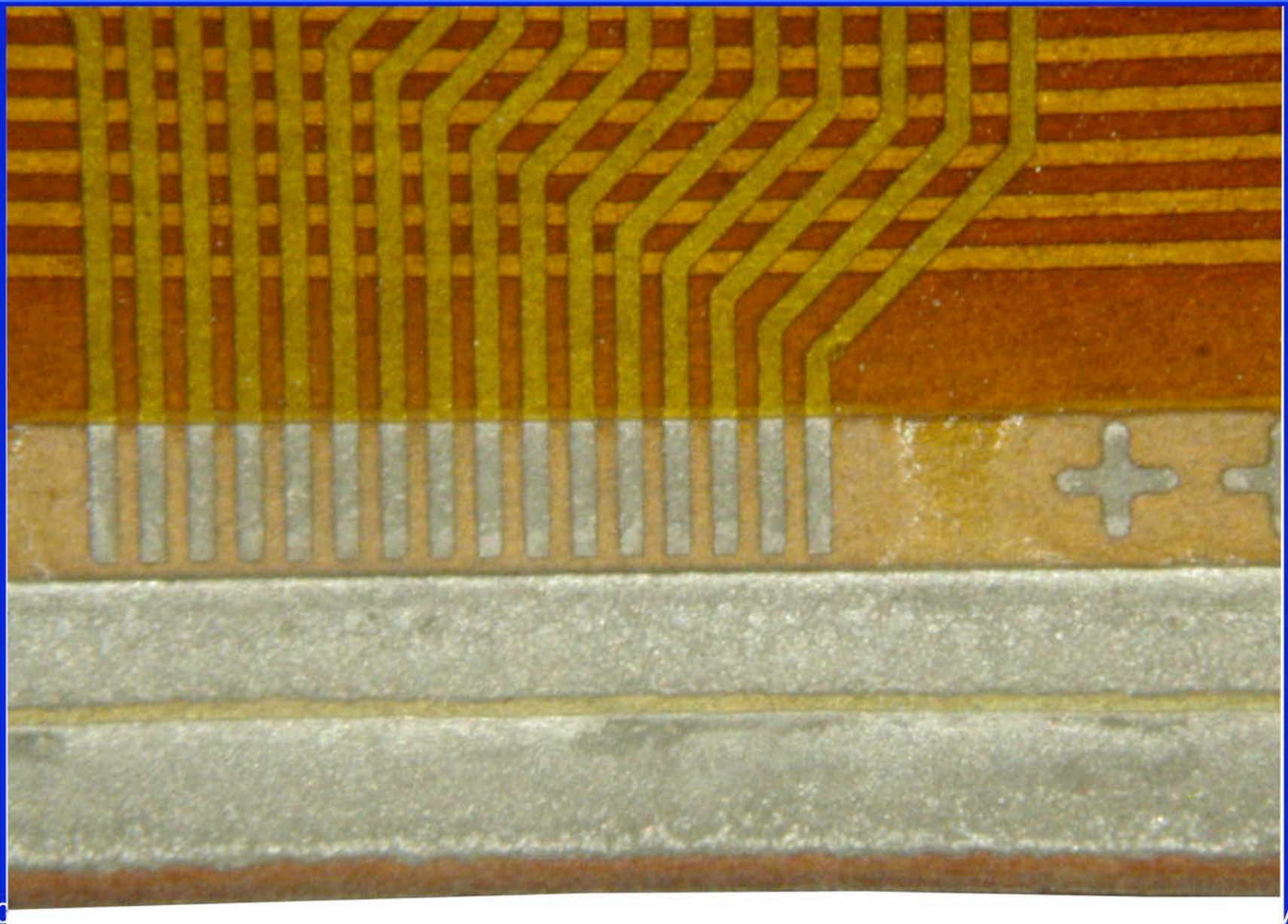
# The pixel bus



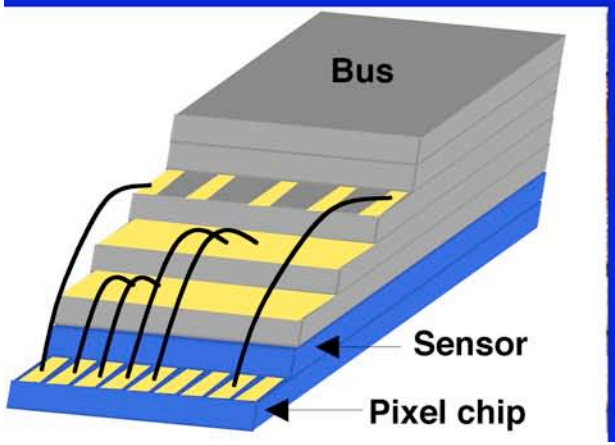



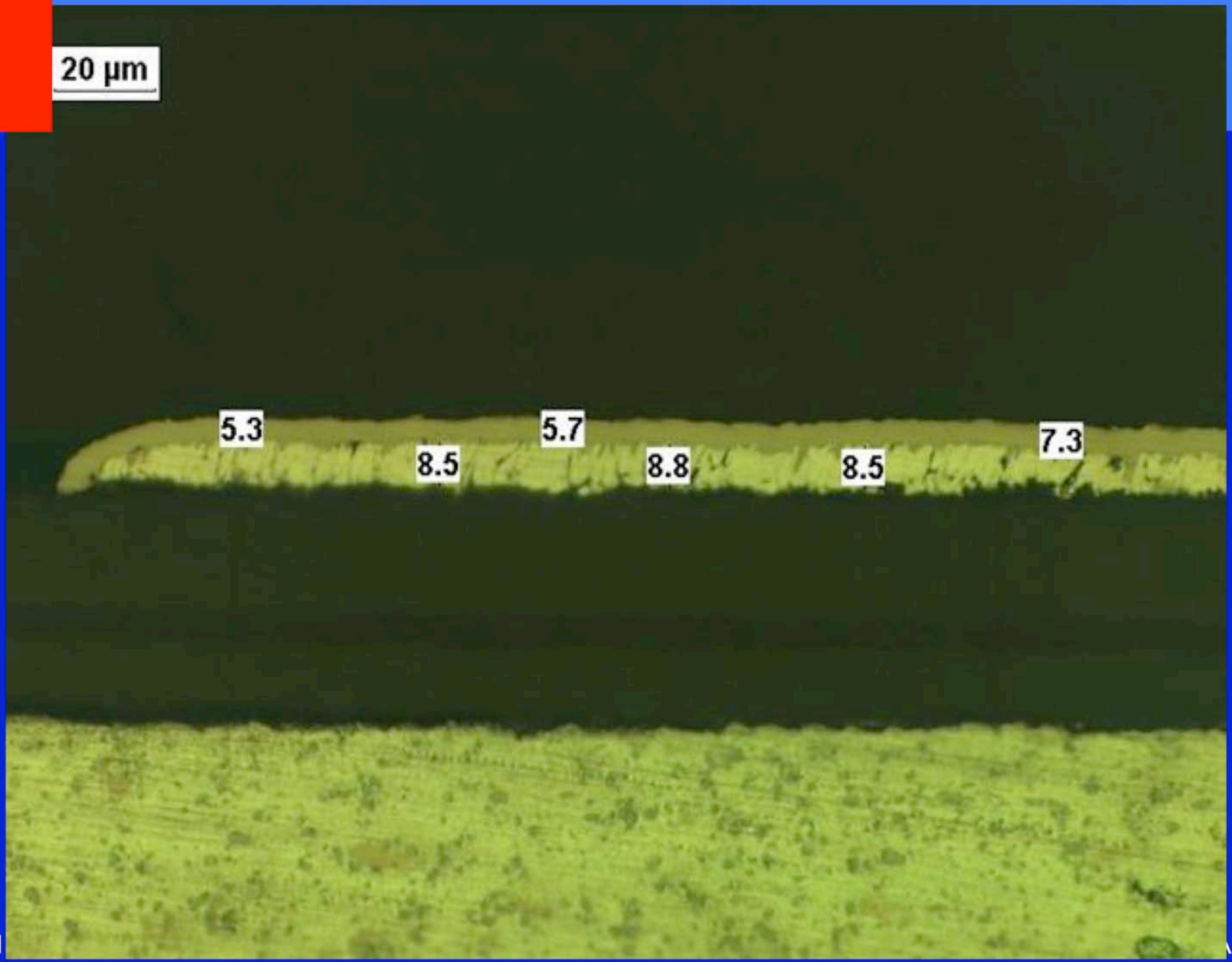
# The pixel bus



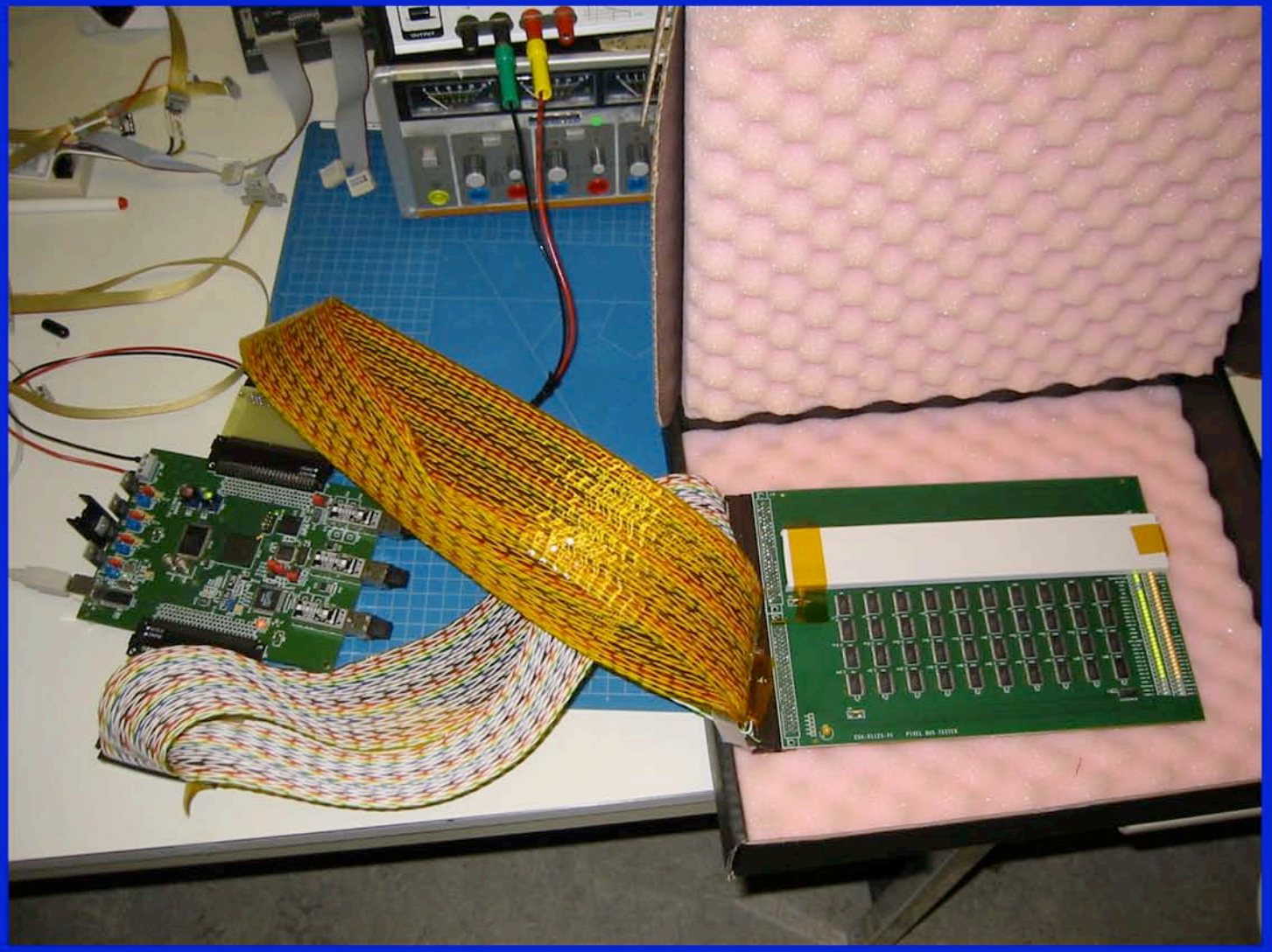
# The pixel bus



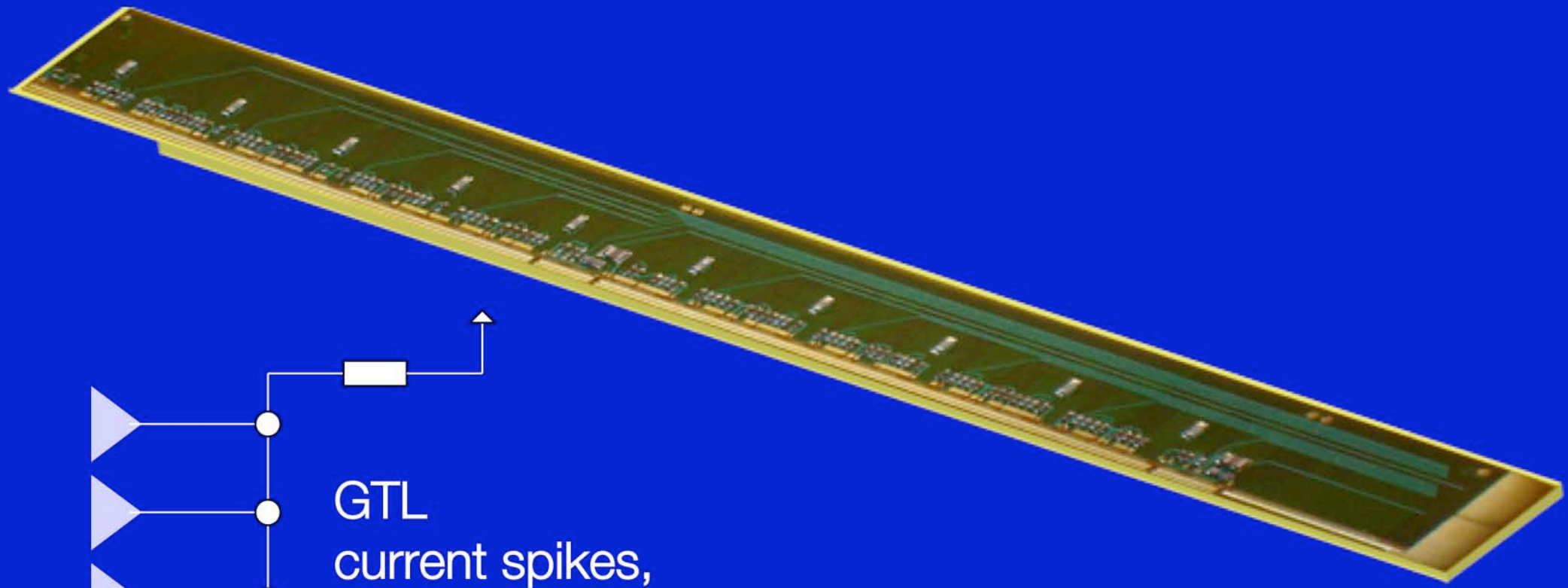

A. Kluge


20 µm
5.3
8.5
5.7
8.8
8.5
7.3

# AI bus



# The pixel bus



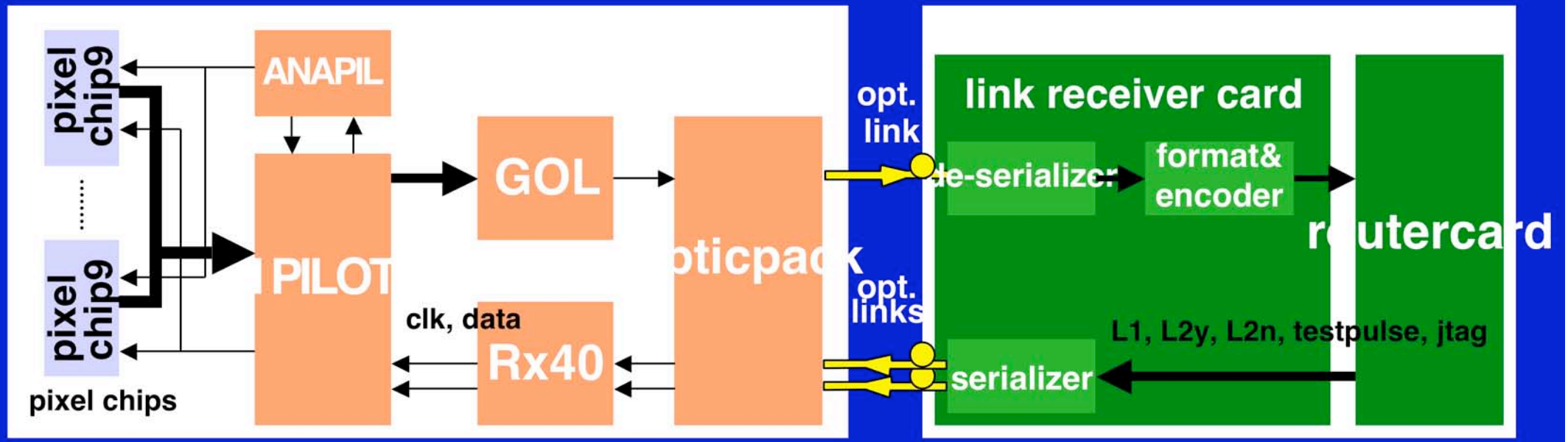


GTL
current spikes,
impedance mismatch
analogue bias lines

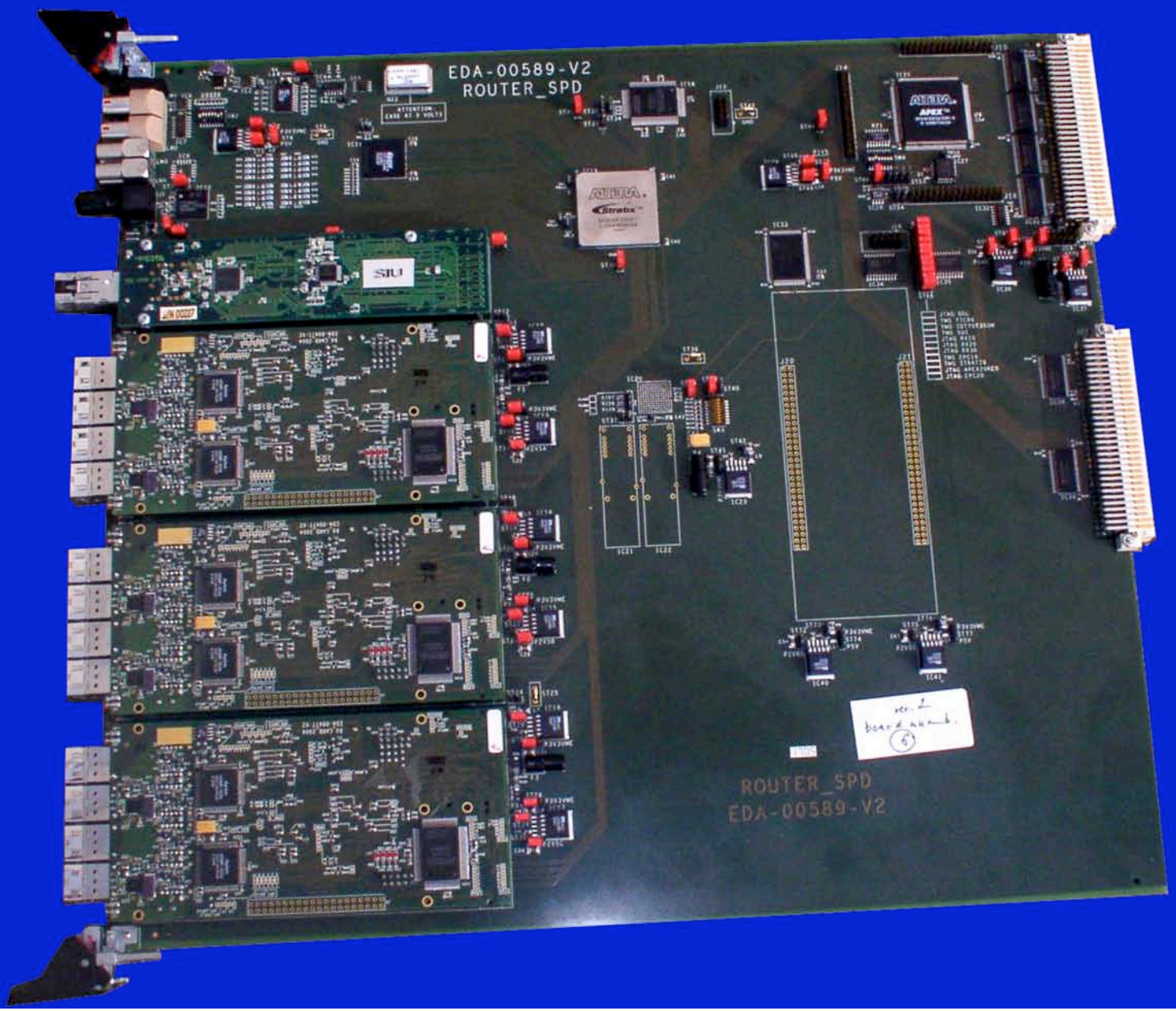
~800 wire bonds
connectivity challenge, reliability

# Off detector electronics

# Off detector electronics



# Off detector electronics

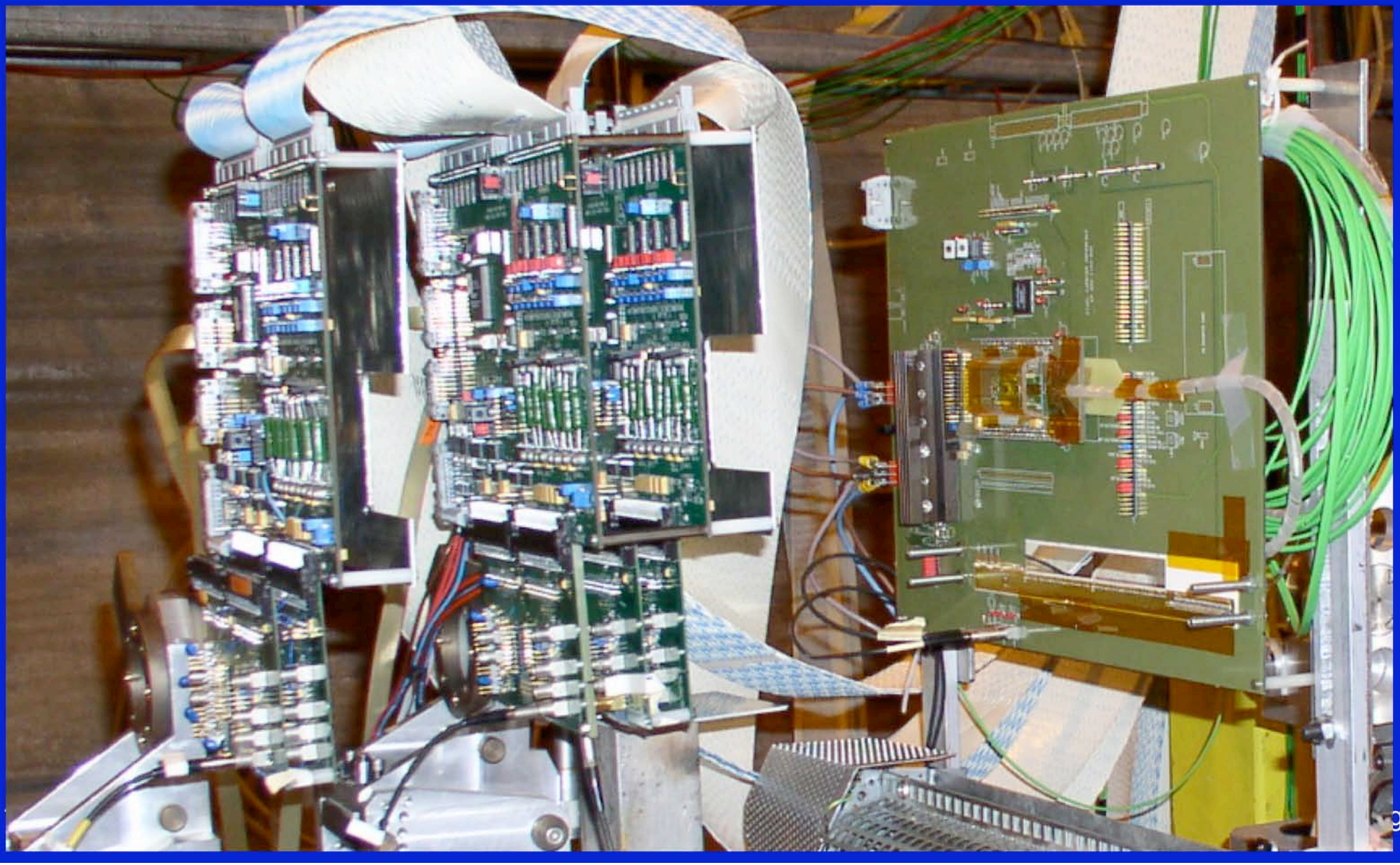


# Pre-installation Integration test

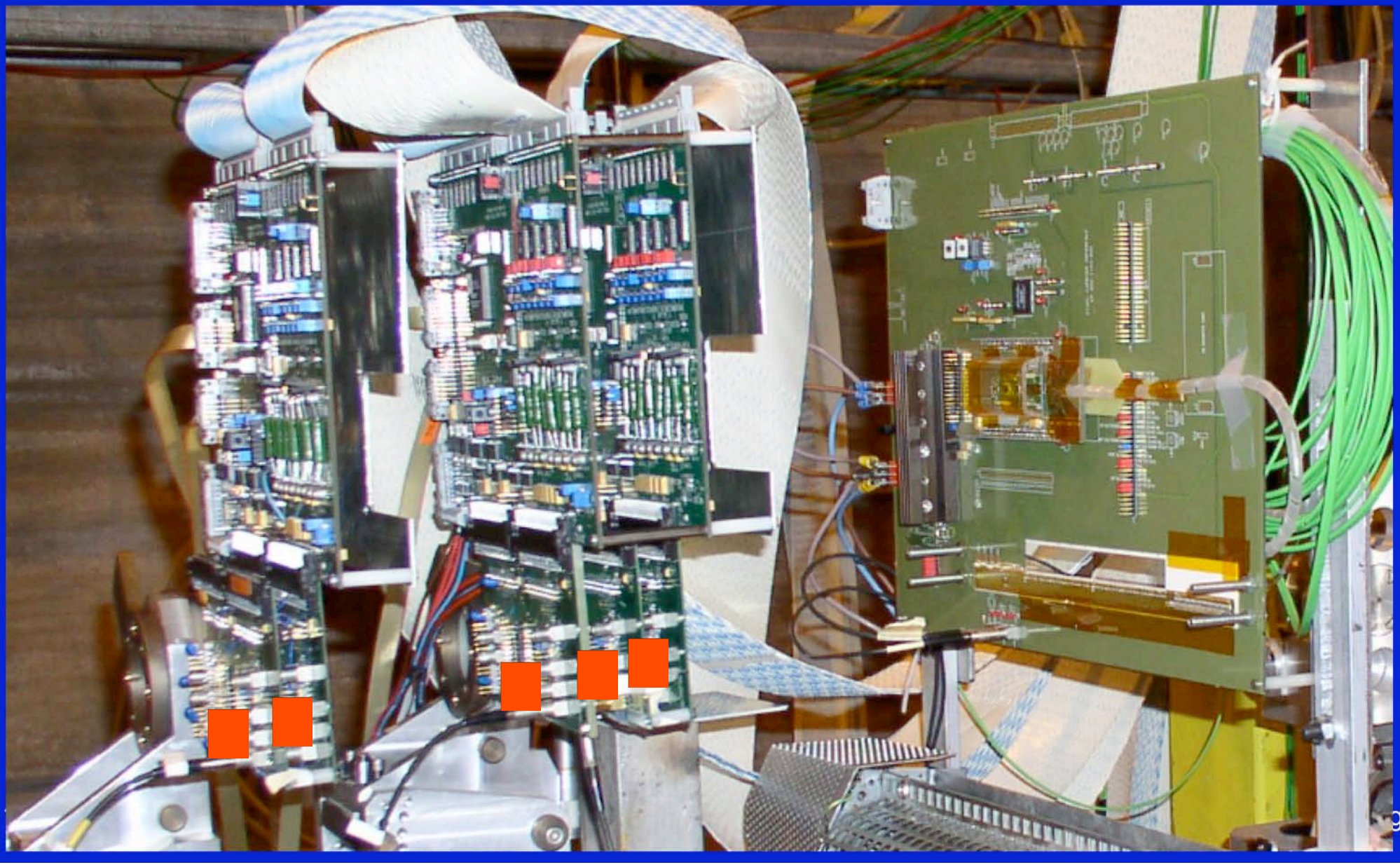


A. Kluge

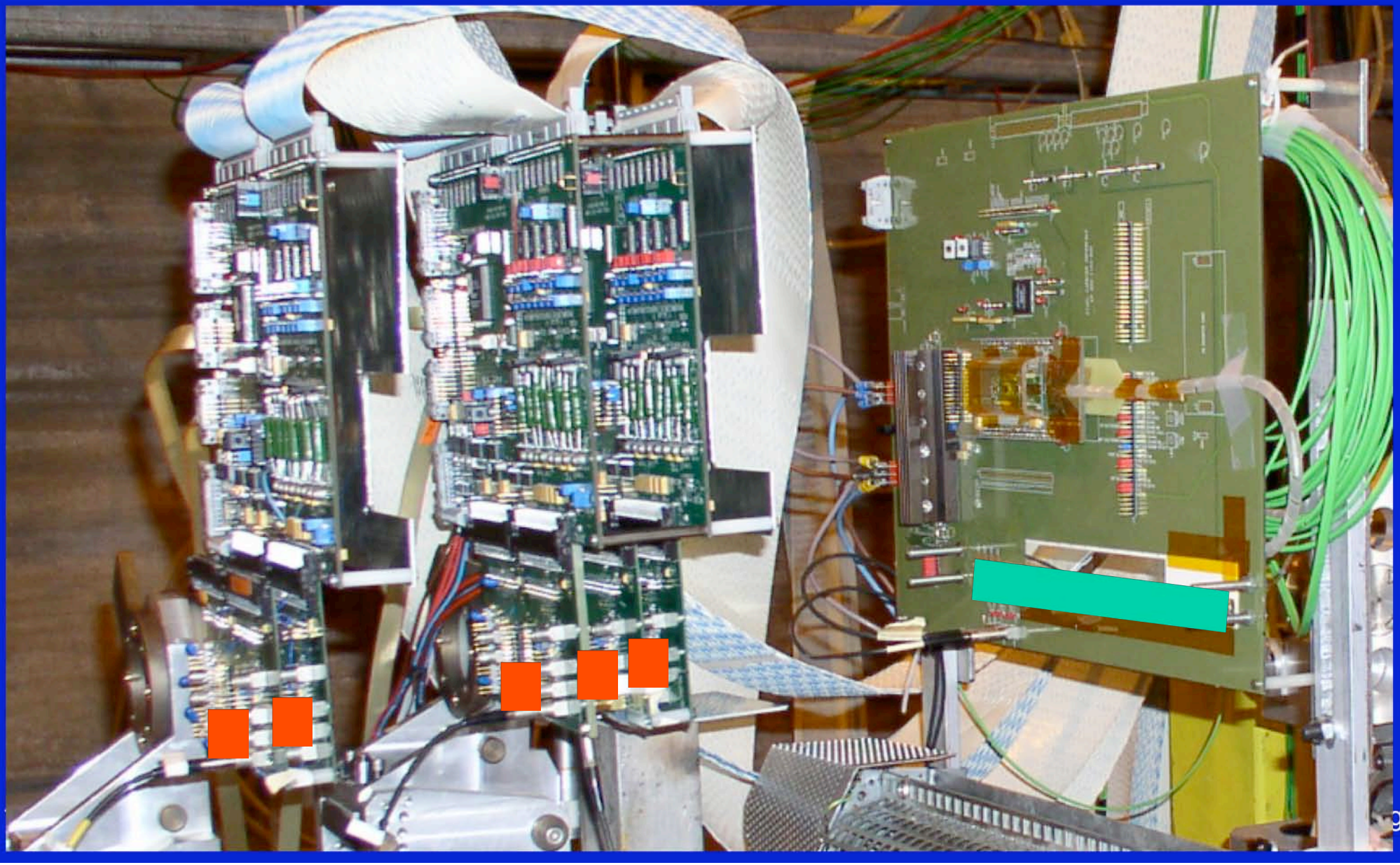
# System test in test beam



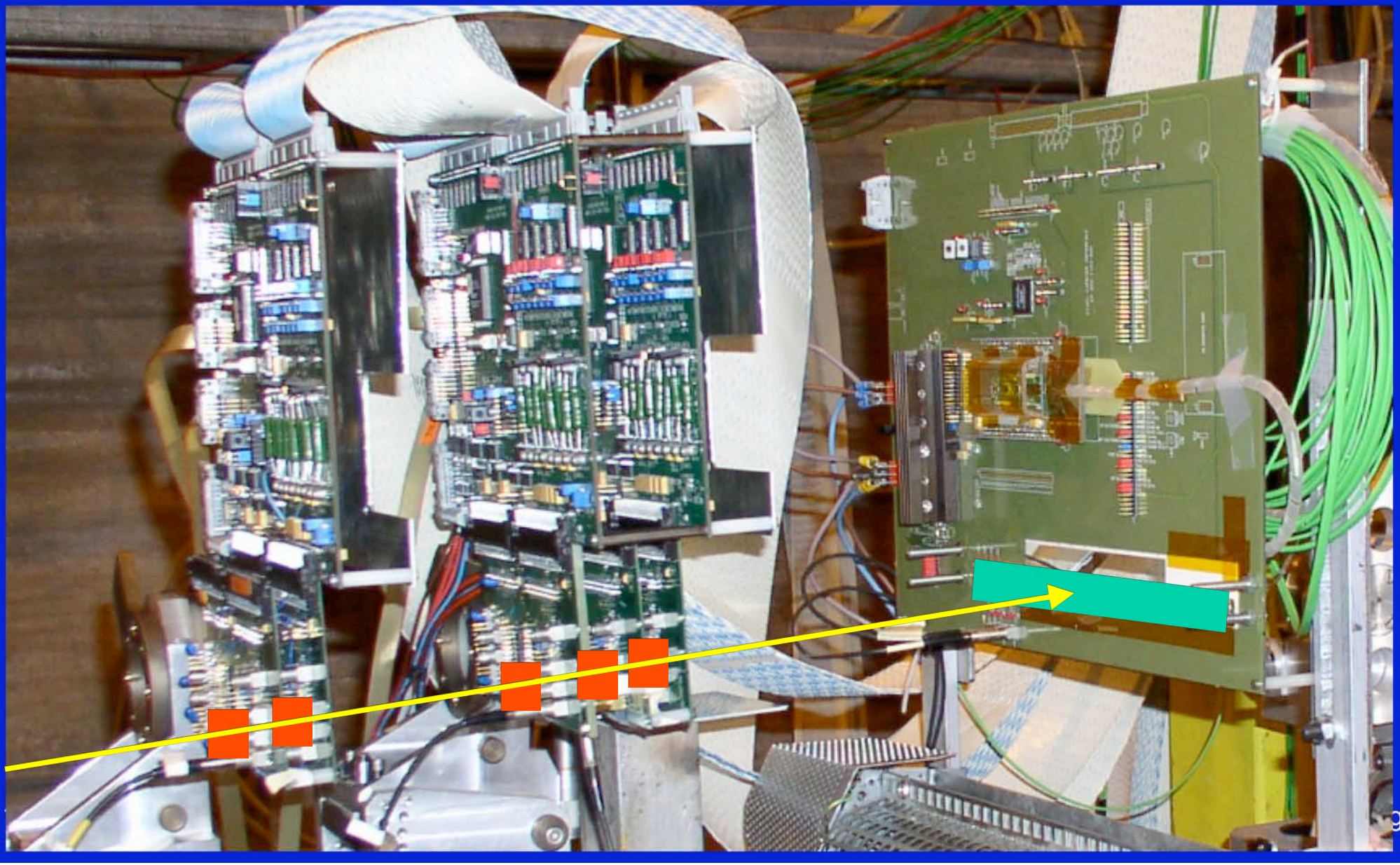
# System test in test beam



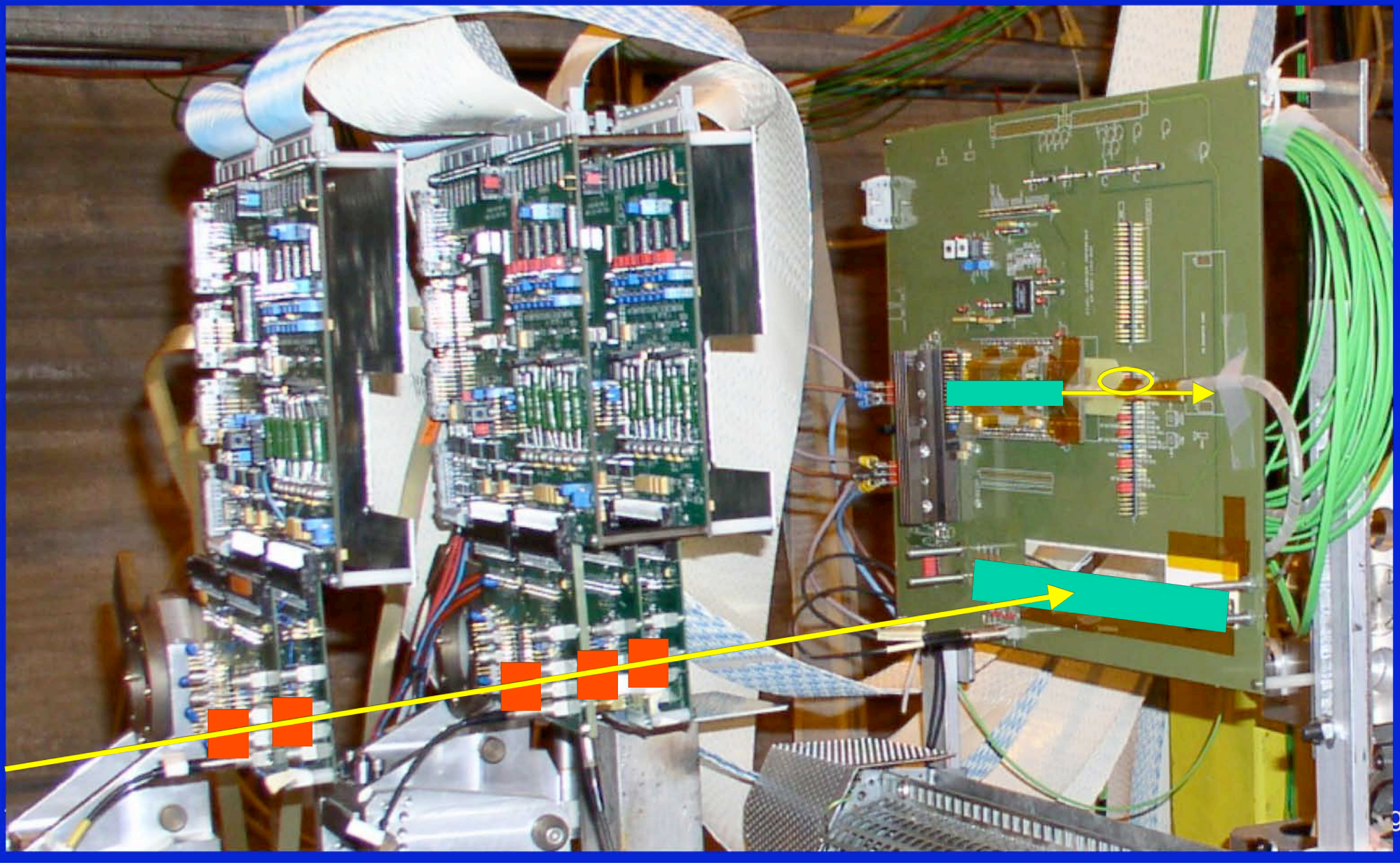
# System test in test beam



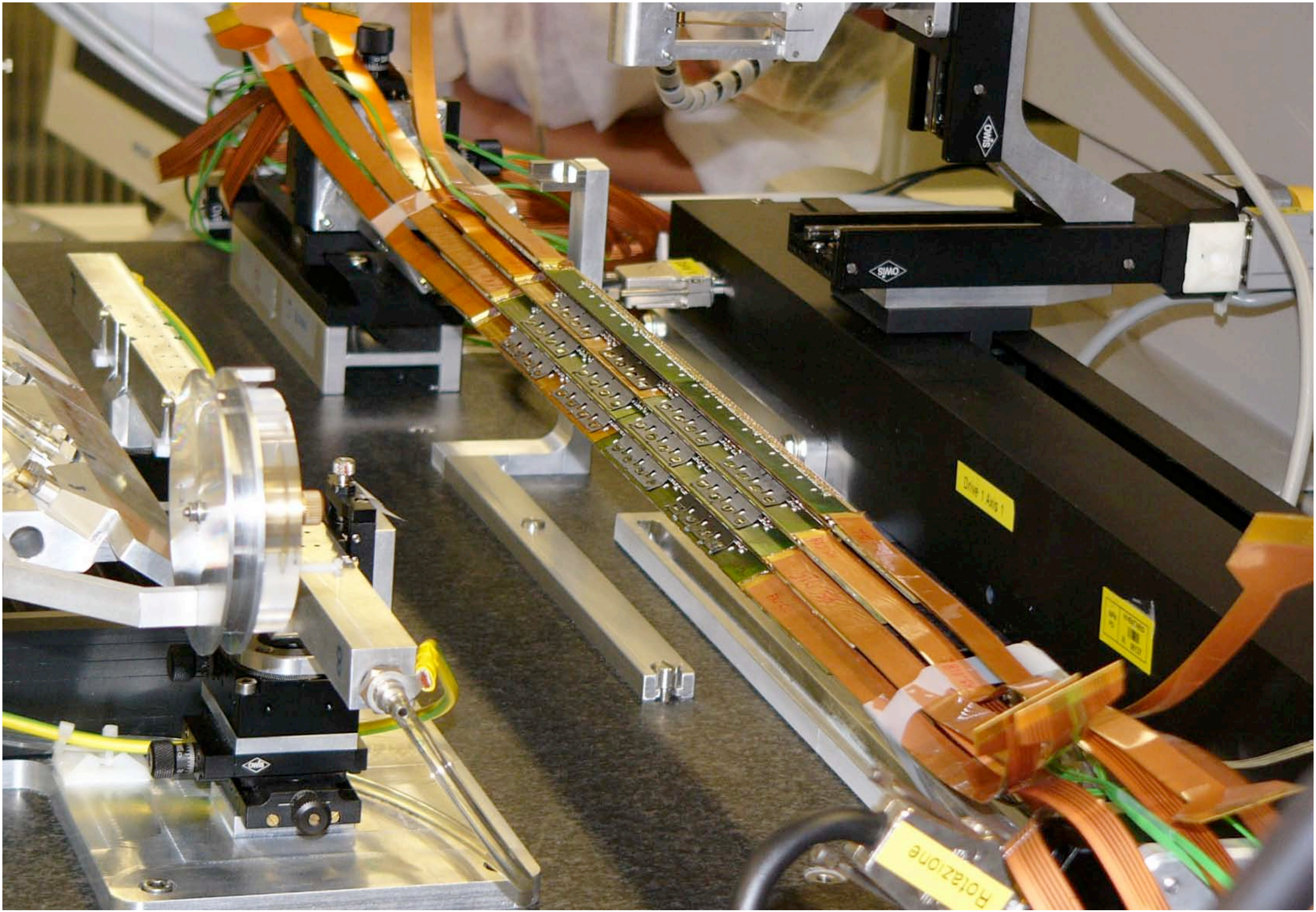
# System test in test beam

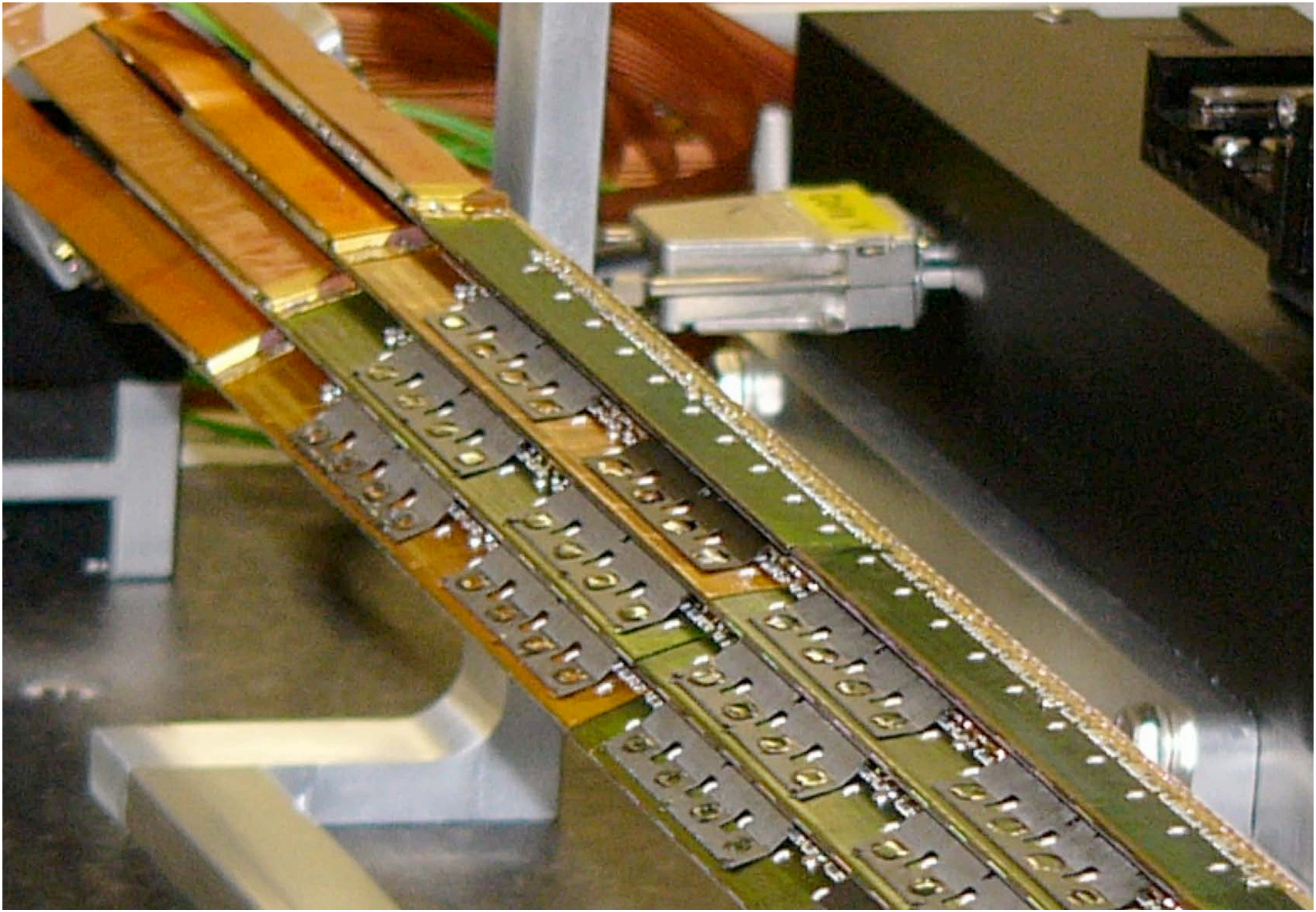


# System test in test beam

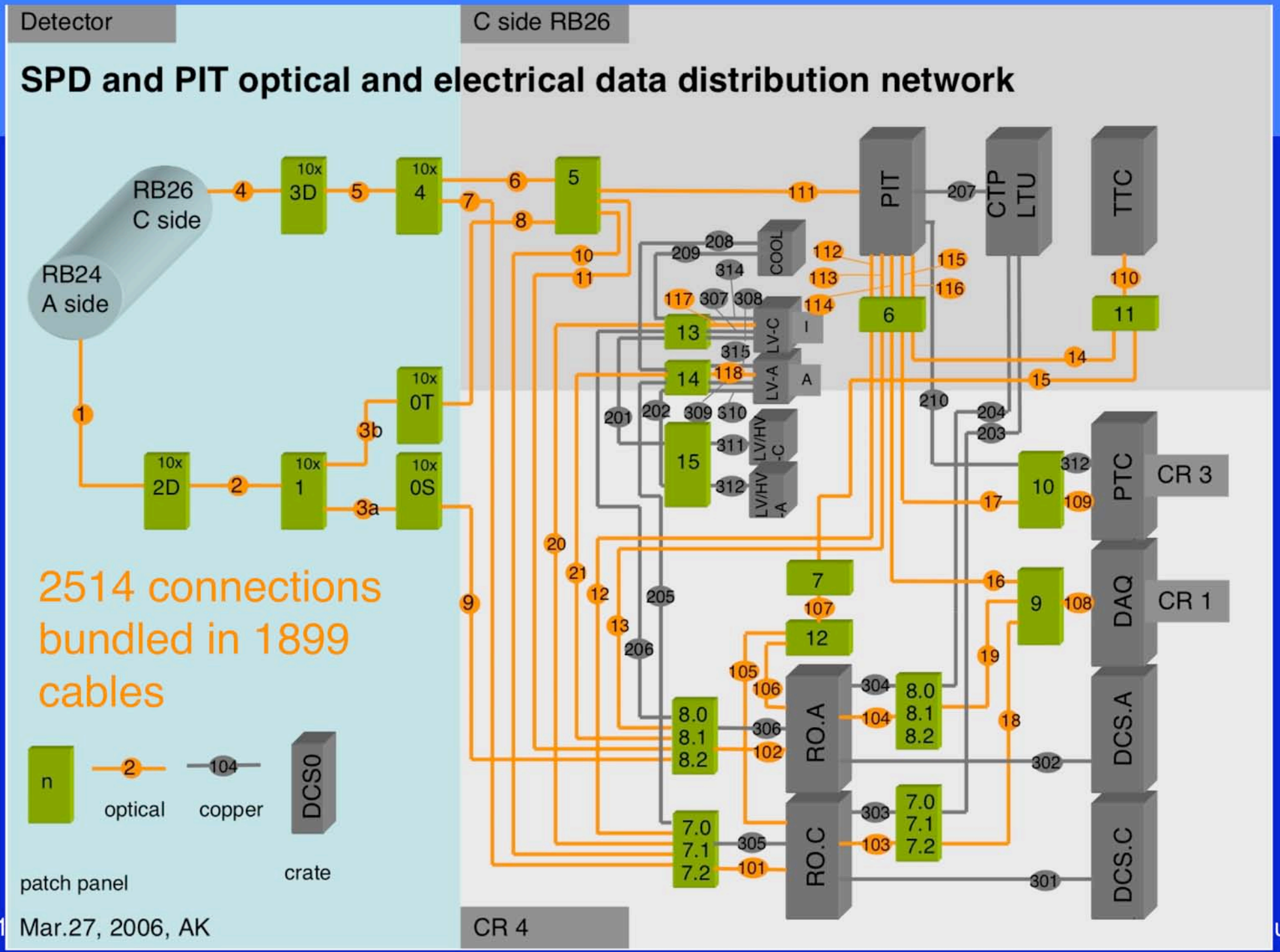


# System and Detector Integration test


Drive 1 Axis 1
Rotazione



# Infrastructure & Cabling

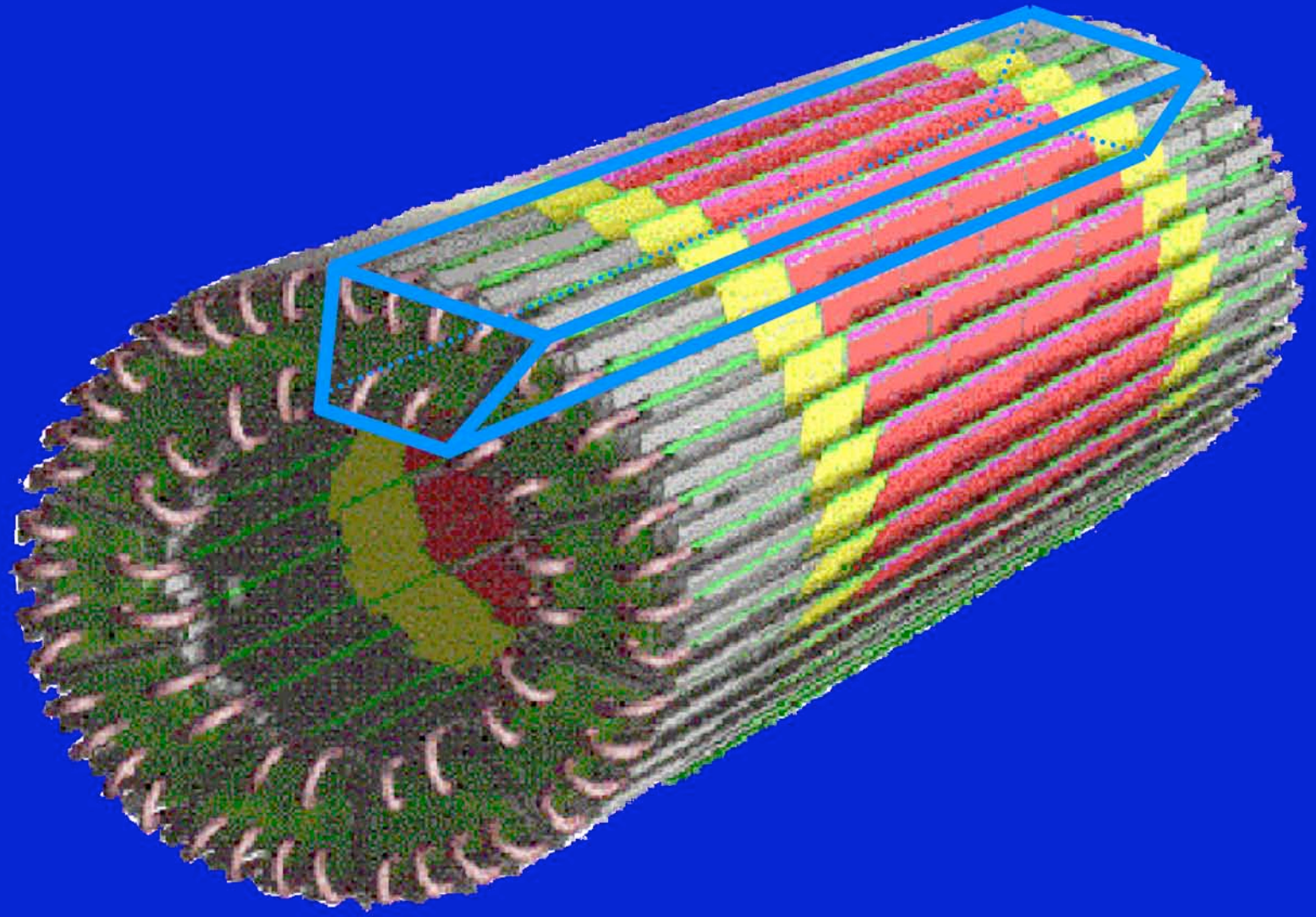

Detector
C side RB26
SPD and PIT optical and electrical data distribution network
RB26
C side
RB24
A side
10x
3D
10x
4
10x
0T
10x
2D
10x
1
10x
0S
PIT
CTP
LTU
TTC
COOL
LV-C
I
LV-A
A
LV/HV
-C
LV/HV
-A
PTC
CR 3
DAQ
CR 1
DCS.A
DCS.C
RO.A
RO.C
8.0
8.1
8.2
7.0
7.1
7.2
2514 connections
bundled in 1899
cables
n
optical
copper
DCS0
patch panel
crate
CR 4
Mar.27, 2006, AK

# L0 pixel trigger

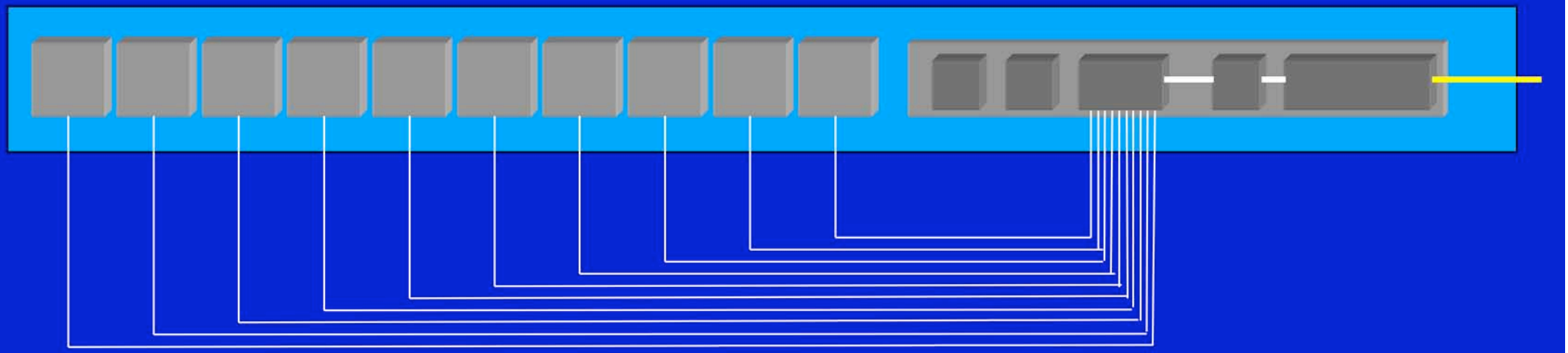


A. Kluge

# SPD

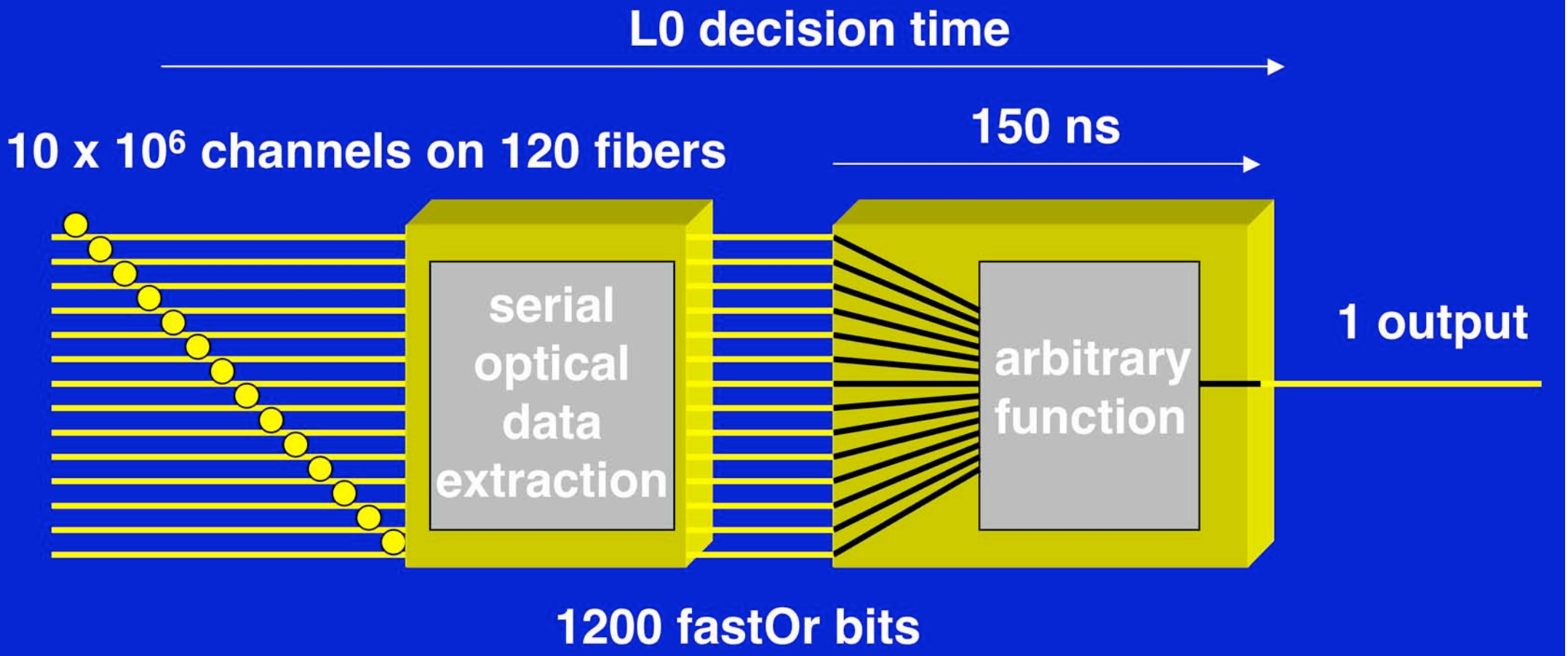


# FastOr generation

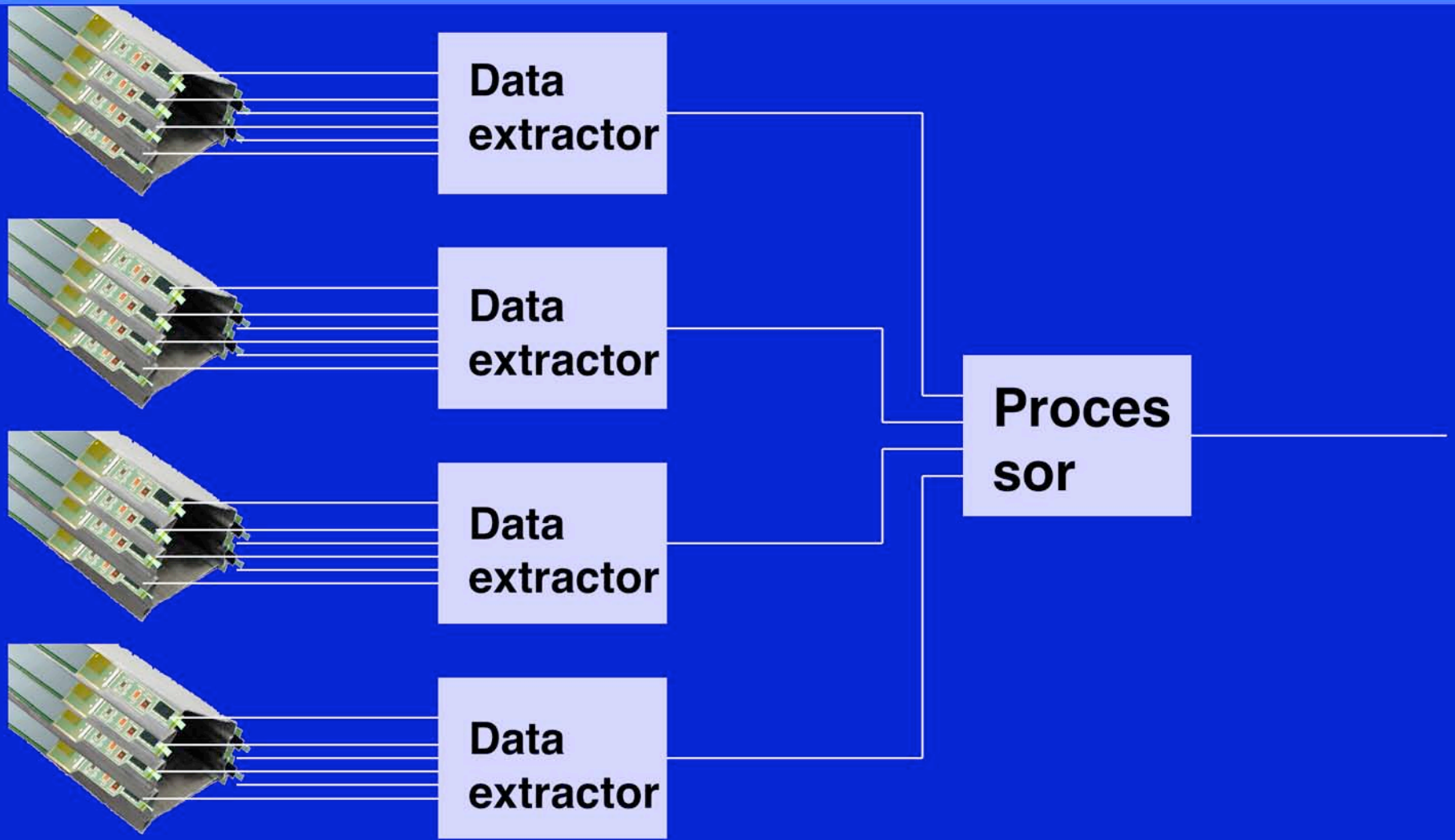


## 120 x half staves each 10 bit fastOr

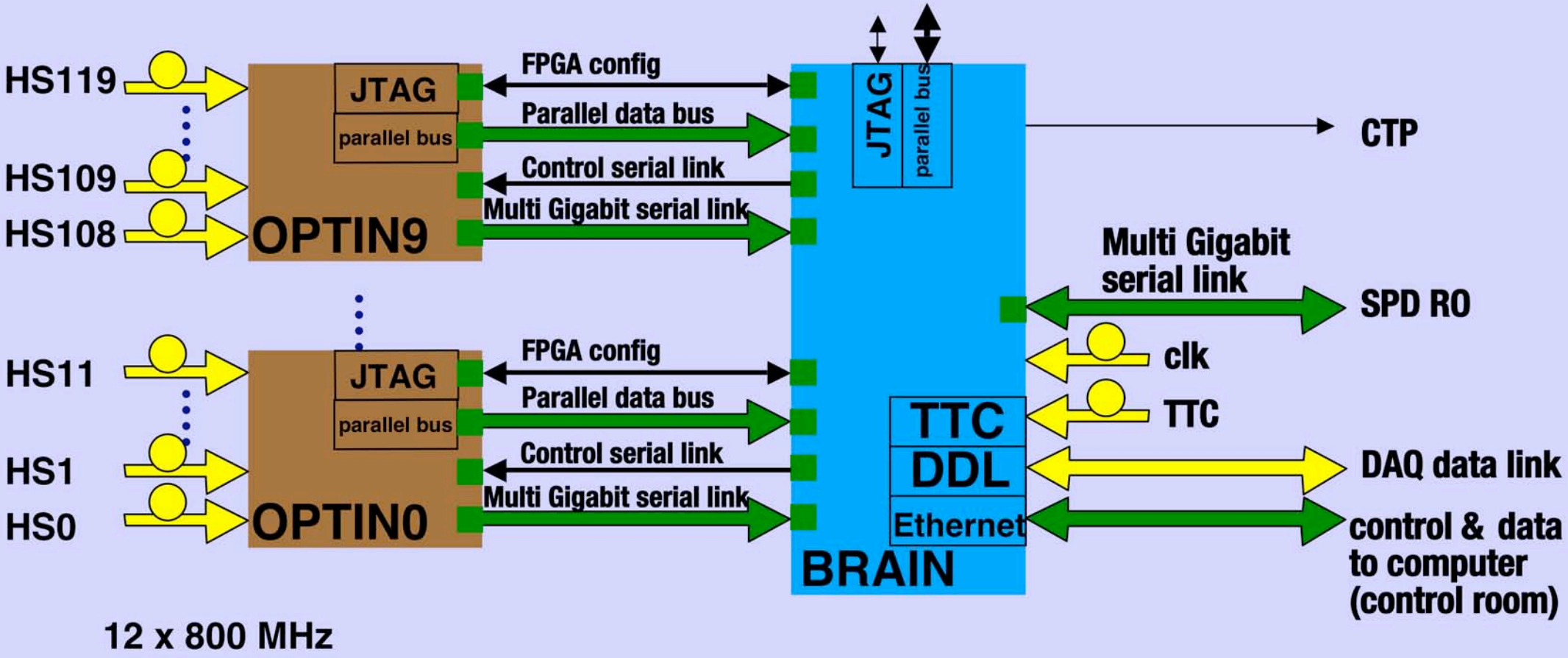
# Pixel trigger



# Architecture



# ALICE pixel trigger processor



# Conclusion

- After a long R&D phase we know how to build this detector and its electroncis
- We have available all electronics components
- 20% of the detector already is available and operating