CMS Pixel Detector: Performance and Prospects towards SLHC

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Outline

- Brief introduction to CMS pixel architecture

- Brief review of architecture inherent data loss mechanisms

- Compare expectations to actual measurements in high rate beam and X-ray box

- Show limitations for very high particle fluences, beyond LHC

- Sketch possible extensions of pixel front end on different levels of complexity according to different levels of particle fluence

Context for this presentation

It is not yet known how the upgraded CMS tracker will look like. Different ideas are around

Will need to replace most of the strip tracker through some kind of pixelated detectors

'Soft' upgrade scenario conceivable (personal believe). LHC probably will not increase luminosity by one order of magnitude in one go. There could be a time with 2-3 times LHC luminosity

Have to replace existent pixel layers due to radiation damage anyway. Can possibly replace by same modules with improved or extended readout chips (very little extra effort)

Improved readout chips could be used as is for outer layers, as a guide to make new architectures or not at all...

CMS Pixel Detector

blade
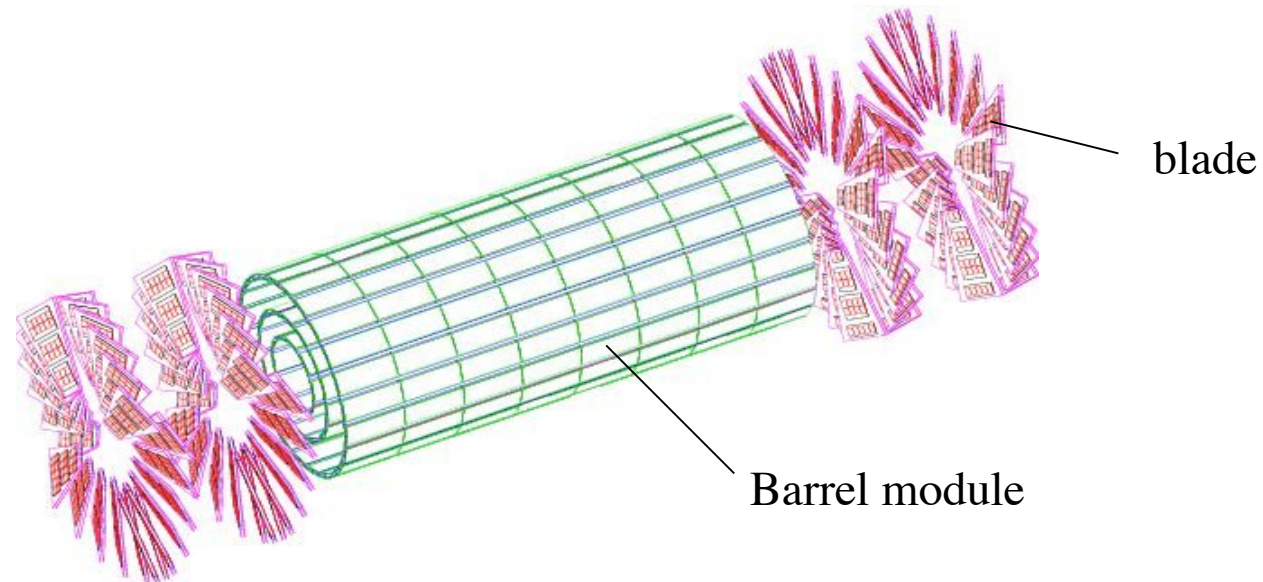
Barrel module

2 endcap disks: z= ±34.5 cm and ±46.5 cm $\qquad$ total area: $0.28m^2$
3 barrel layers: r≈ 4.3, 7.2 and 11 cm $\qquad$ total area: $0.78m^2$

Mean pixel fluence for inner disks: $\qquad$ 31 MHz/cm^2
$\qquad$ for 4cm barrel layer: $\qquad$ 115MHz/cm^2

Barrel Module

Kapton signal cable

Power/bias cable

3 layer HDI
$7\mu m$ Cu, $10\mu m$ Kapton

TBM (Token Bit Manager chip)

Sensor 64.8x16.2mm^2
n-in-n, p-spray
Pixel size 150x100μm^2

8x2 readout chips PSI46V2
Bump bonded to sensor
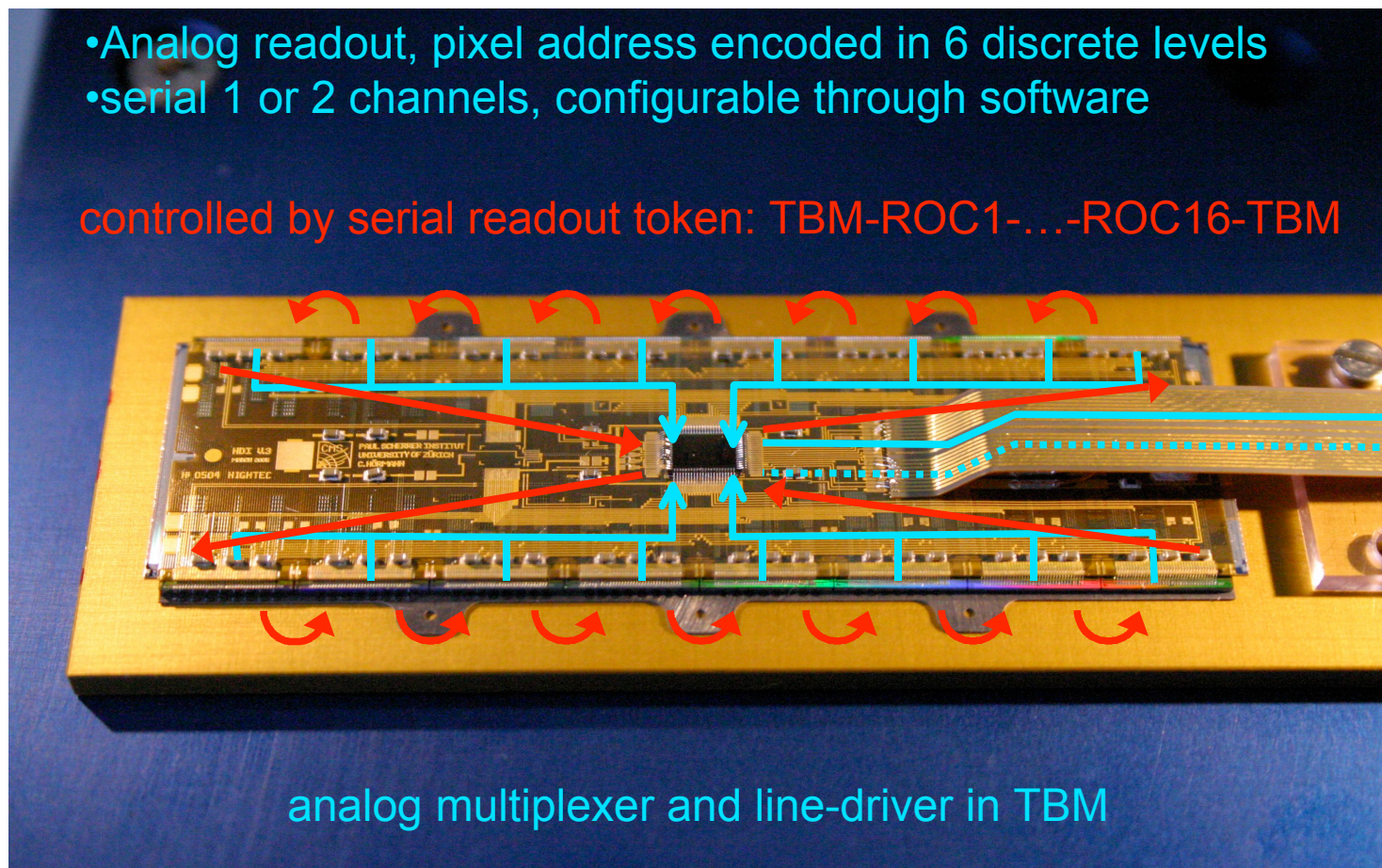
Si_3N_4 Baseplates
Very robust, excellent CTE match to Si
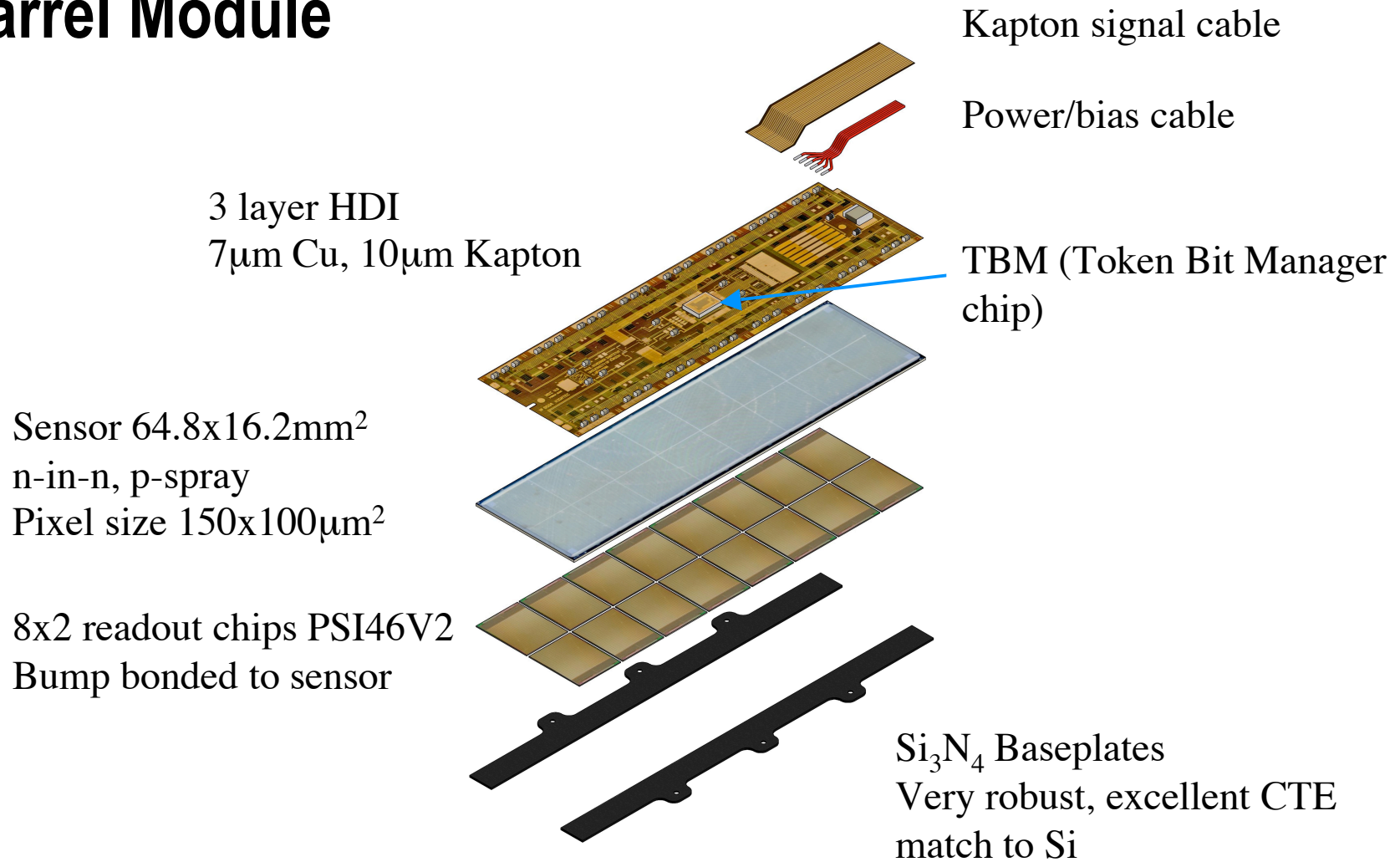
Module readout scheme

- Analog readout, pixel address encoded in 6 discrete levels
- serial 1 or 2 channels, configurable through software

controlled by serial readout token: TBM-ROC1-…-ROC16-TBM

analog multiplexer and line-driver in TBM

Readout Chip PSI46V2

0.25 mm technology

Pixel size $100\times150\mu m^2$
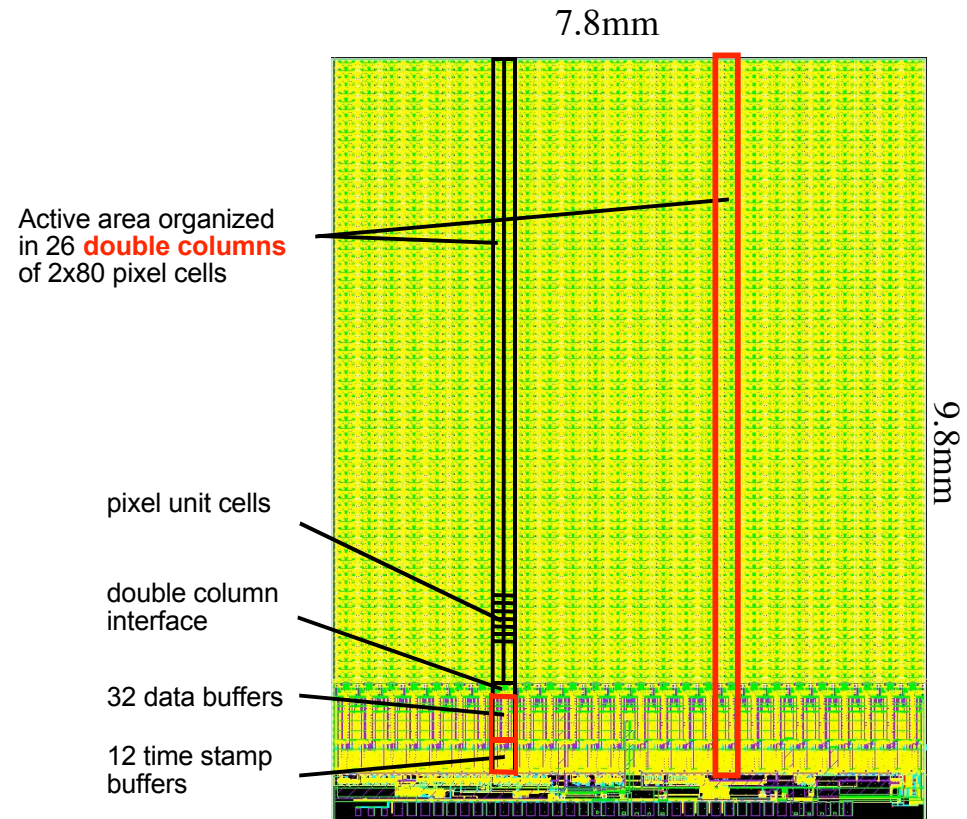
4160 pixels in array of 52x80

Pixels organized in double columns.

Column drain architecture
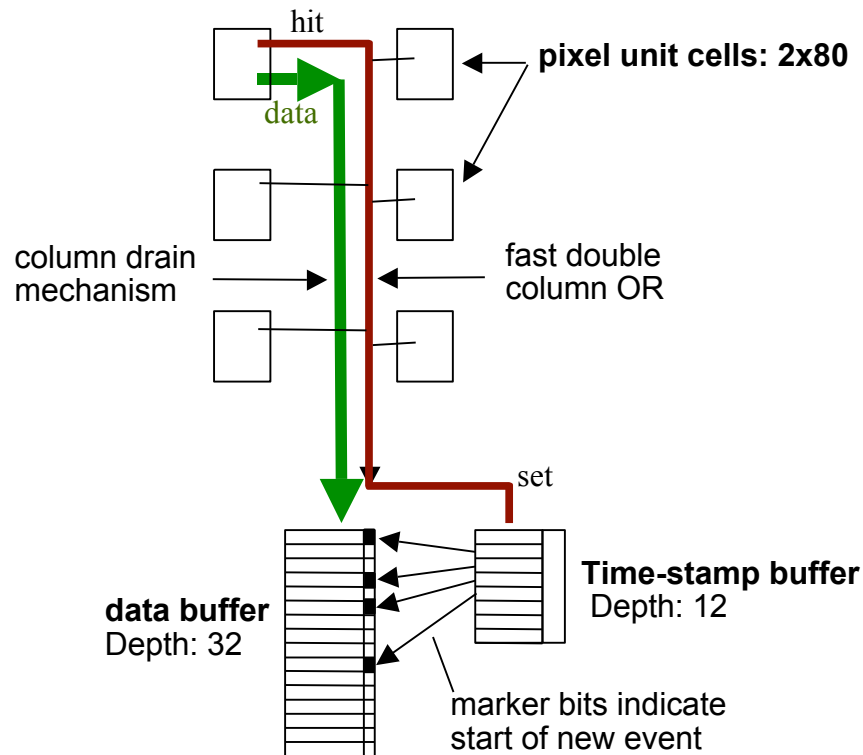
Size of double column periphery: $900\mu m$. **Mainly due to time stamp and data buffers ($800\mu m$)**

Chip periphery contains voltage regulators, fast I^2C interface, 28 DACs for chip settings

7.8mm

9.8mm

Active area organized in 26 **double columns** of 2x80 pixel cells

pixel unit cells

double column interface

32 data buffers

12 time stamp buffers

Column drain architecture

sketch of a double column

hit

data

pixel unit cells: 2x80

column drain
mechanism

fast double
column OR

set

data buffer
Depth: 32

Time-stamp buffer
Depth: 12

marker bits indicate
start of new event

- Zero suppression in pixel cell

- Pixel hit information transferred to time stamp and data buffers

- Kept there during L1 trigger latency

- Double column stops data aquisition when confirmed L1 trigger
  ⇒ dead time

- Double column resets after readout
  ⇒ loosing history (trigger latency)

- Serial readout: Controlled through readout token passing from chip to chip and double column to double column. Chips daisy chained 8 (16) ROCs.

Data loss mechanisms

Pixel busy:
0.04% / **0.08%** / **0.21%**
pixel insensitiv until hit
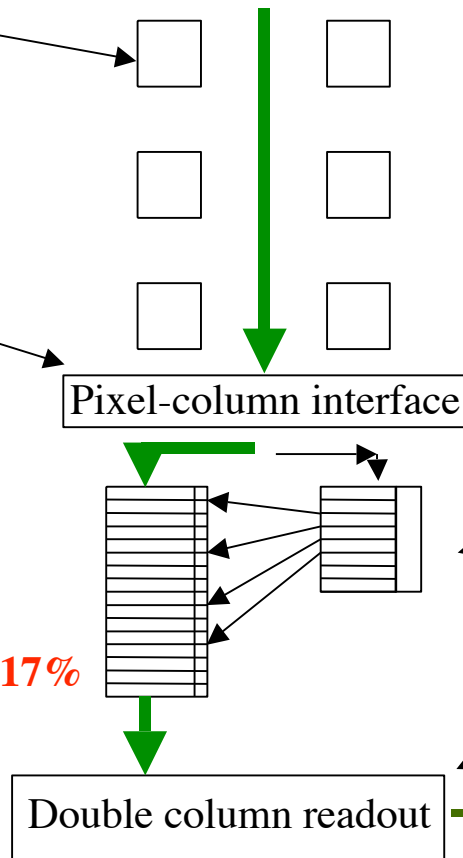transferred to data buffer
(column drain mechanism)

Double column busy:
0.004% / **0.02%** / **0.25%**
Column drain transfers hits
from pixels to data buffer.
Maximum 3 pending column
drain requests accepted

Data Buffer full:
0.07% / **0.08%** / **0.17%**

Pixel-column interface

Double column readout

- **1xLHC: 10^{34}cm^{-2}s^{-1}**
- **11 cm** / **7 cm** / **4 cm layer**
- **total data loss @ 100kHz L1A:**
  - **0.8%**
  - **1.2%**
  - **3.8%**

Timestamp Buffer full:
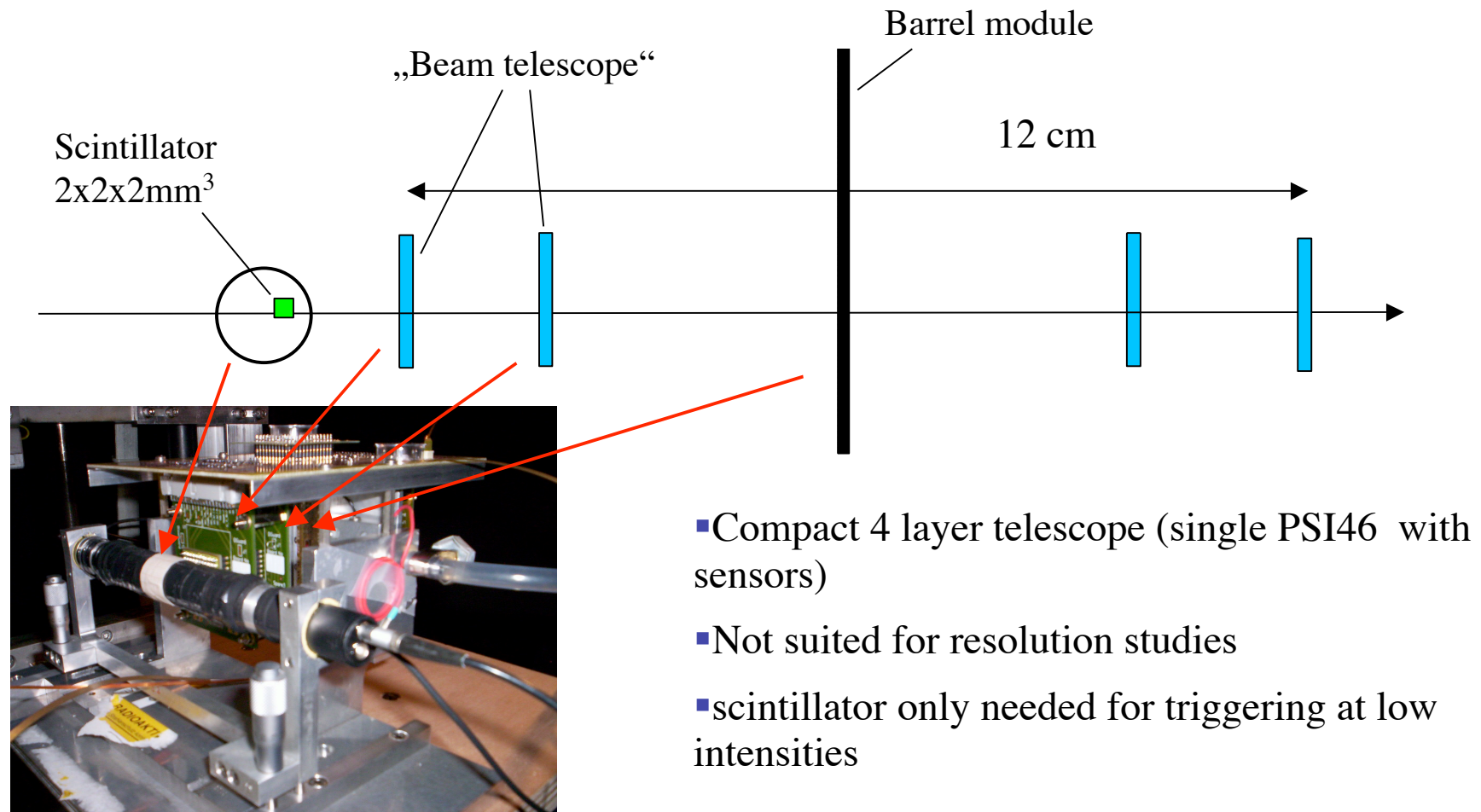**0** / **0.001%** / **0.17%**

Readout losses:
0.7% / **1%** / **3.0%**
for 100kHz L1 trigger rate
Column is blocked after L1A and
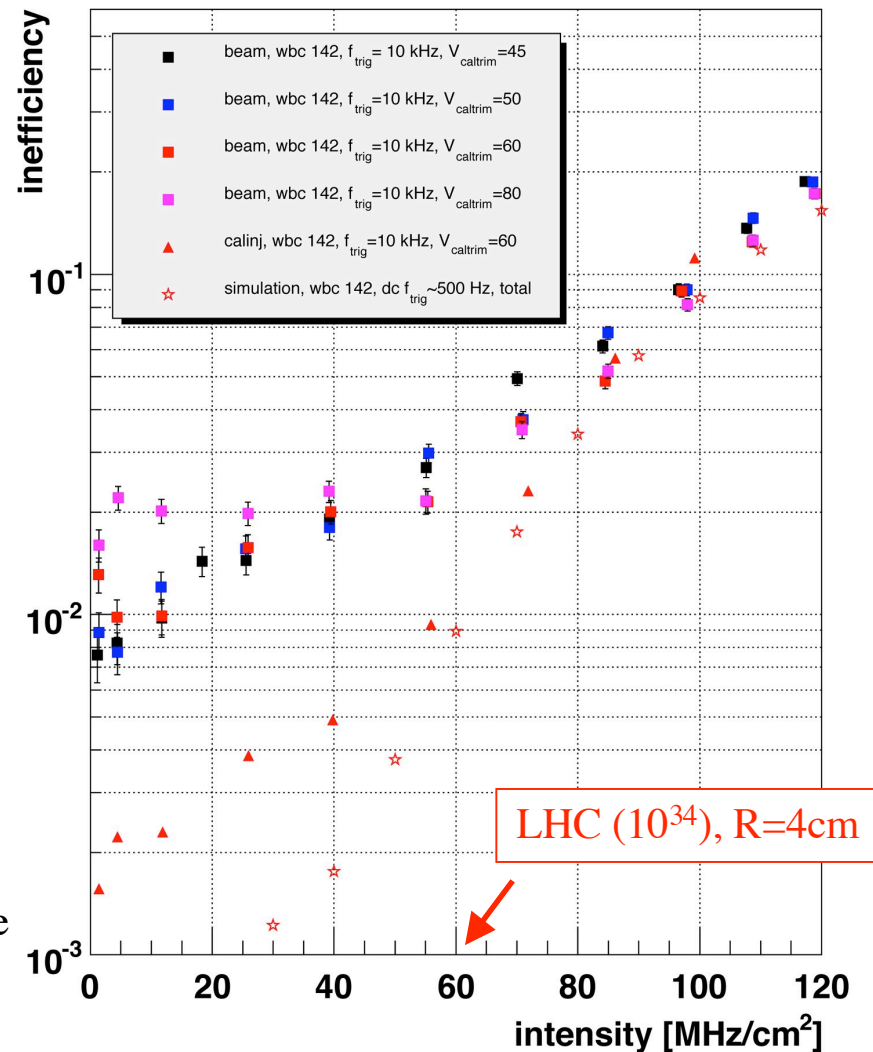reset when read out

Testbeam measurements @ PSI

- 300 MeV/c π^+ ~ MIPs,
  but too much multiple scattering for resolution studies

- variable intensity, up to 100 MHz/cm^2
  illumination of a **full module**

- 50 MHz beam structure (close enough to LHC)

  - chips could run at 50 MHz, but peaking time not adequate

  - operate module on synchronized 40 MHz clock

  - allow triggers only every 4th bunch (CMS: ≥ 3 separation)

- no B-field

  - smaller clusters, no 1:1 translation of intensities btw beam and LHC

Testbeam measurements @ PSI

Barrel module

„Beam telescope"

Scintillator
$2 \times 2 \times 2 \text{mm}^3$

12 cm

- Compact 4 layer telescope (single PSI46 with sensors)

- Not suited for resolution studies

- scintillator only needed for triggering at low intensities

Measured inefficiency

- Plot shows
  - Simulation
  - Beam measurements for different thresholds (~2200-4200 electrons)
  - Measurements with calibration pulse injection on top of beam induced activity
- Good agreement for high intensities
- For low intensities: pions show 1-2% more inefficiency than expected from simulation
- Cal injects agree fairly well O(0.1%)
- Sensor effects?
  - Radiation damage? (module has seen 0.5×10^{14} pions)
  - Bump yield ?
  - Ongoing measurements with new module indicate ~0.2% inefficiency at low intensity (2MHz/cm^2)

Legend:
- beam, wbc 142, f_{trig}= 10 kHz, $V_{caltrim}$=45
- beam, wbc 142, f_{trig}=10 kHz, $V_{caltrim}$=50
- beam, wbc 142, f_{trig}=10 kHz, $V_{caltrim}$=60
- beam, wbc 142, f_{trig}=10 kHz, $V_{caltrim}$=80
- calinj, wbc 142, f_{trig}=10 kHz, $V_{caltrim}$=60
- simulation, wbc 142, dc f_{trig}~500 Hz, total

LHC (10^{34}), R=4cm

inefficiency vs intensity [MHz/cm^2]

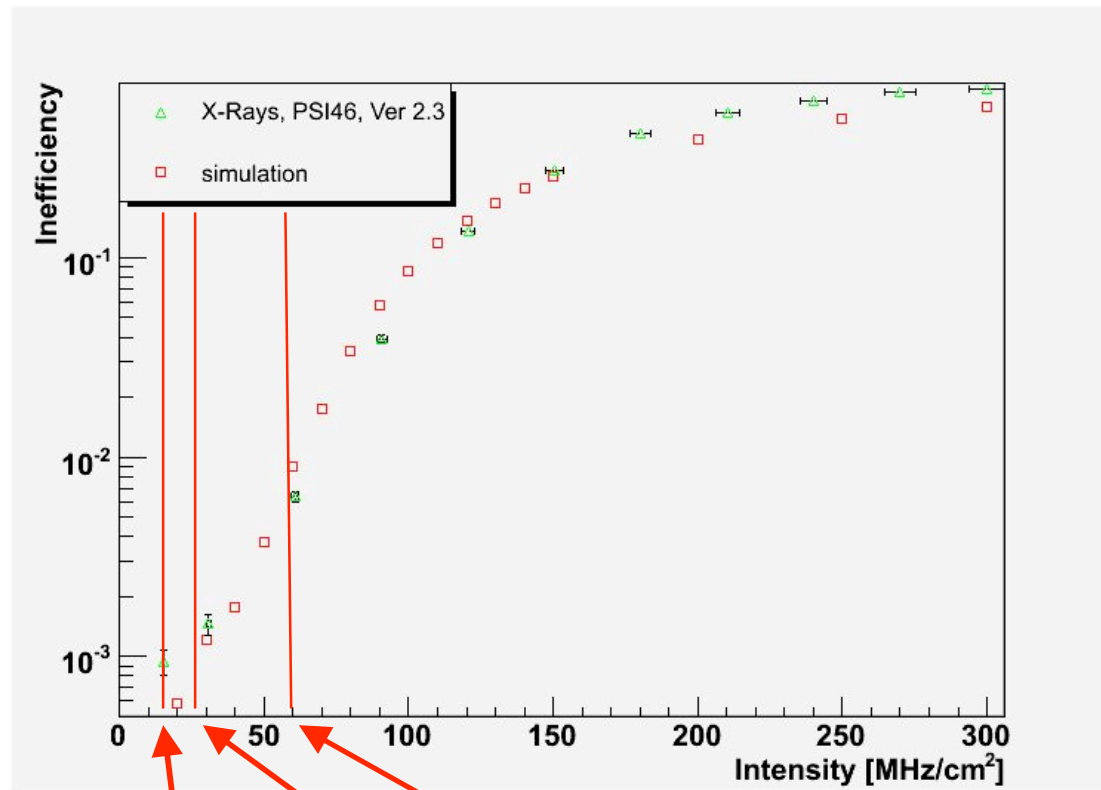# Beyond LHC: measurement in X-ray box

- Very high photon fluence up to 300MHz/cm^2

- Single chip sensor

- No TBM

-> short readout times, readout losses negligible (see later)

Simulation agrees very well with measurement
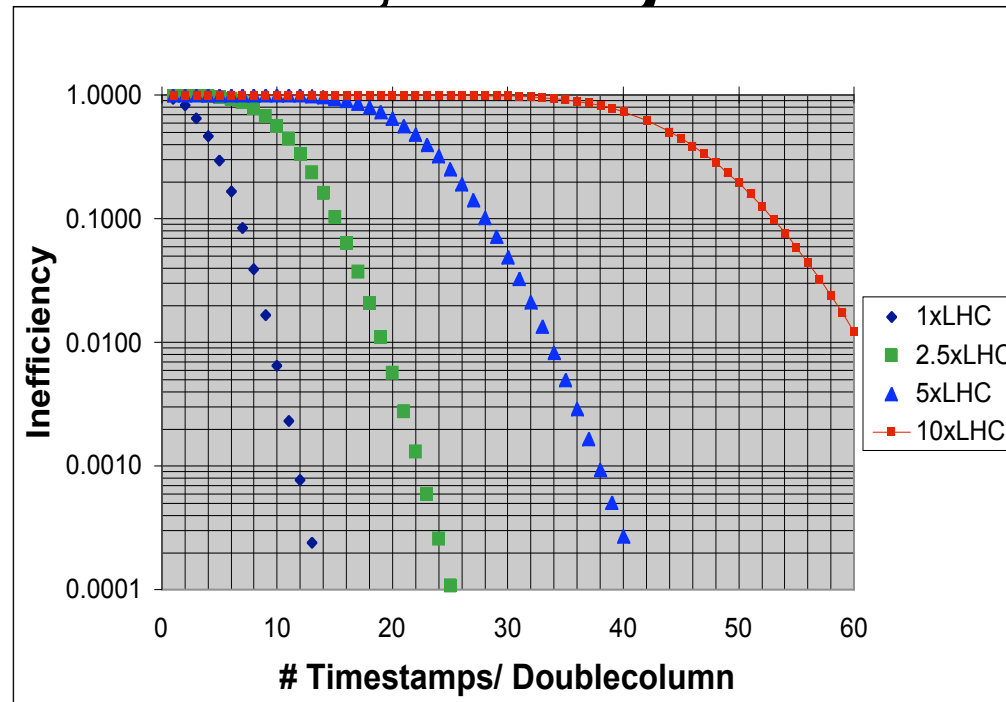

LHC (10^{34}cm^{-2}s^{-1}): 11cm 7cm 4cm

Contributions to data loss

■Entirely dominated by
timestamp buffer overflows

■In experiment also data
buffer overflow (higher pixel
multiplicity)

■Steep rise of inefficiency
due to buffer limitations

■Extension of buffer sizes is
trivial (no R&D)
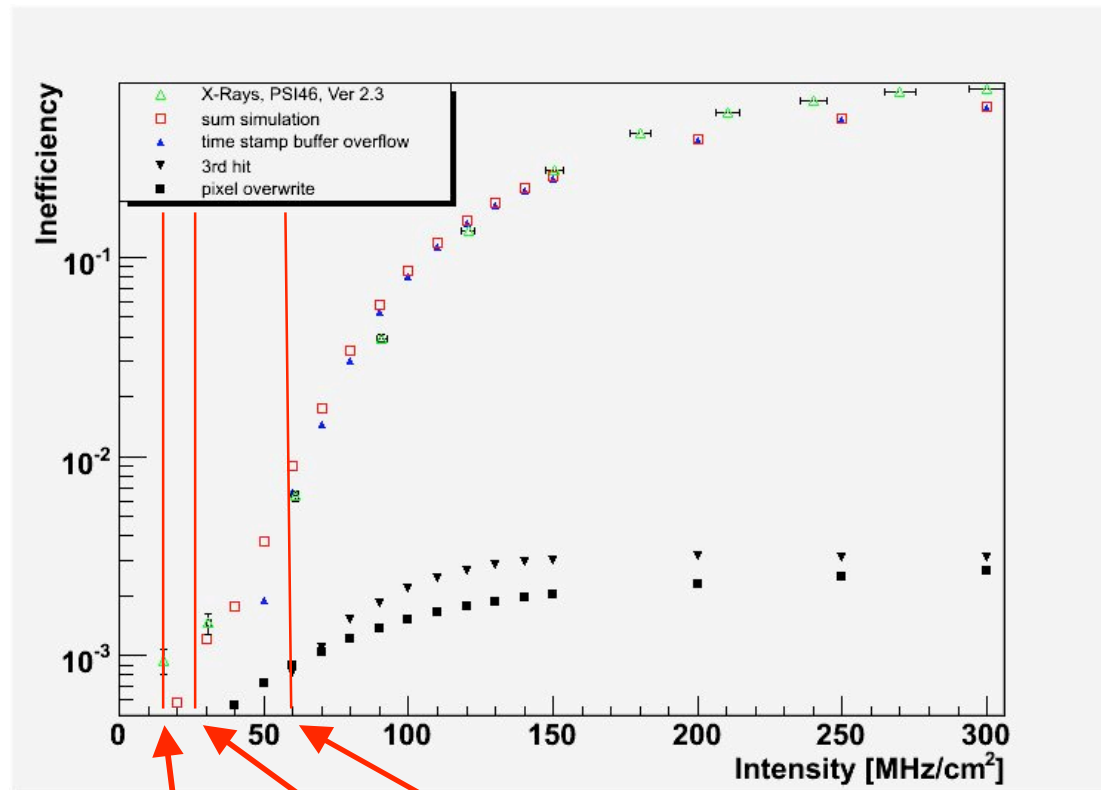
LHC (10^{34}cm^{-2}s^{-1}):   11cm   7cm   4cm

Influence of buffer size, 4cm layer

- Present system: 12 time stamp buffers, 32 data buffers. Average pixel multiplicity:2.2

- For $2.5 \times 10^{34} cm^{-2} s^{-1}$ need to double buffer sizes

- For $10 \times 10^{34} cm^{-2} s^{-1}$ would need 60 timestamp buffers and 190 data buffers (average pixel multiplicity: 2.6).

Enlarging the chip periphery

maximum ROC size

mounting screw whole

0.4mm
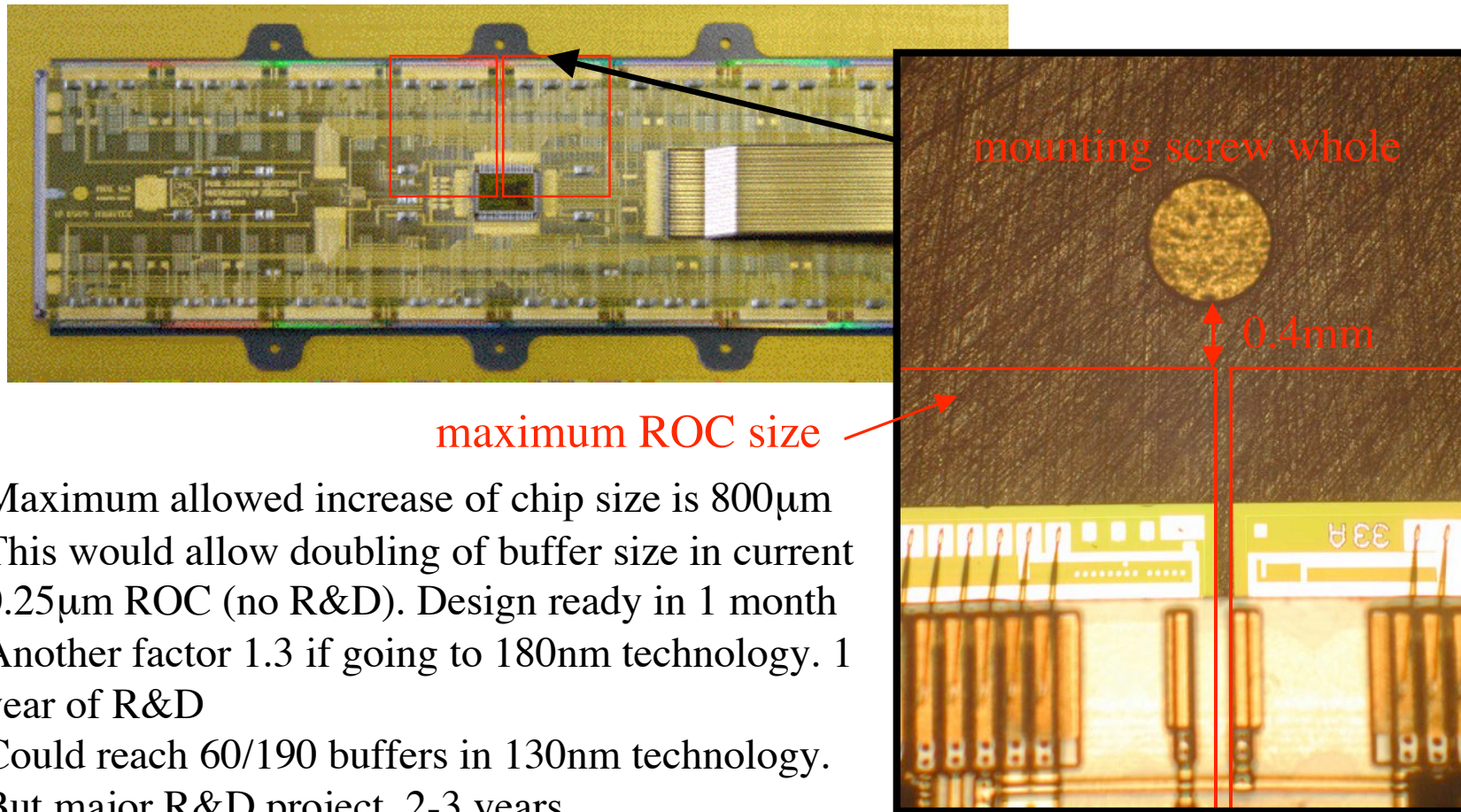
Maximum allowed increase of chip size is 800μm
This would allow doubling of buffer size in current
0.25μm ROC (no R&D). Design ready in 1 month
Another factor 1.3 if going to 180nm technology. 1
year of R&D
Could reach 60/190 buffers in 130nm technology.
But major R&D project. 2-3 years

Other inefficiencies for 4cm layer

Simulations without buffer limitations
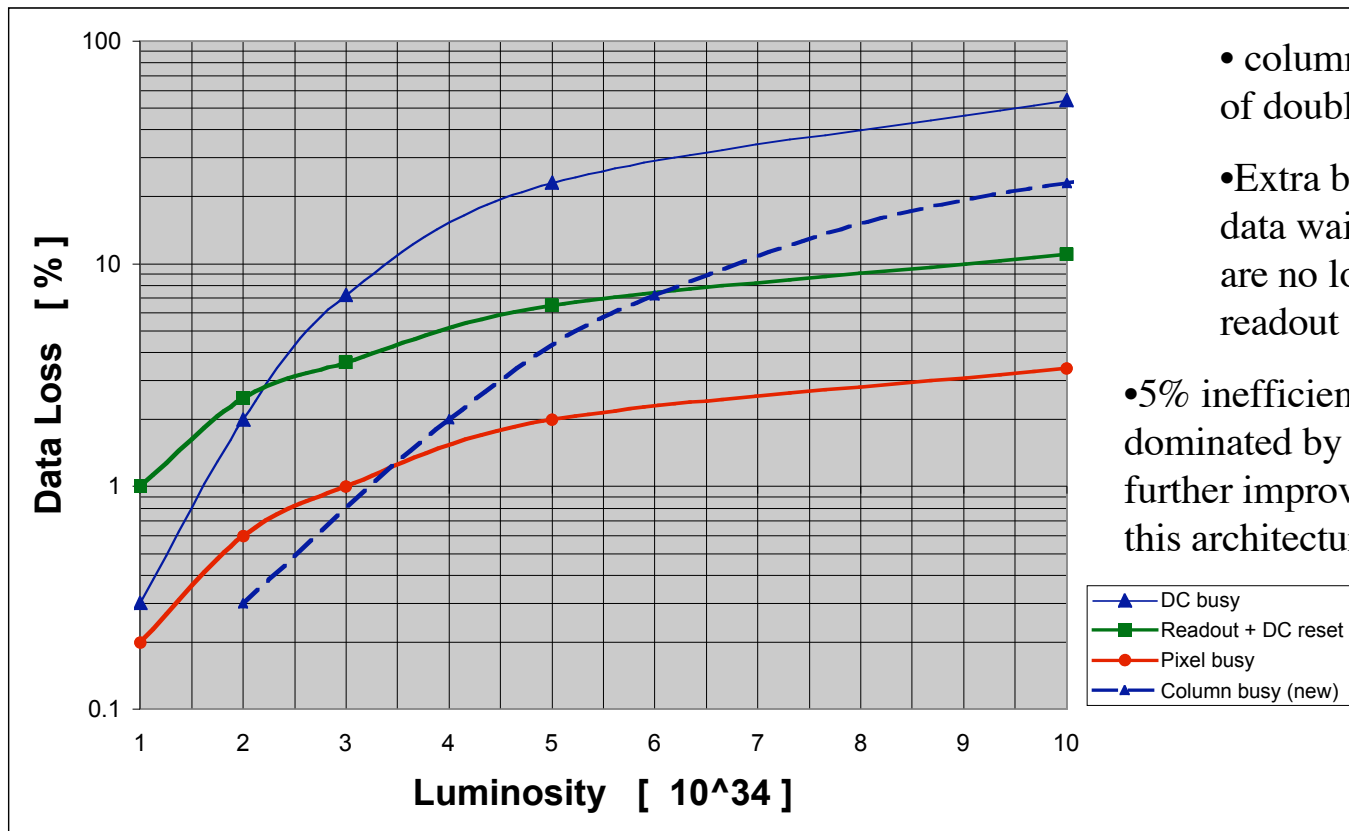
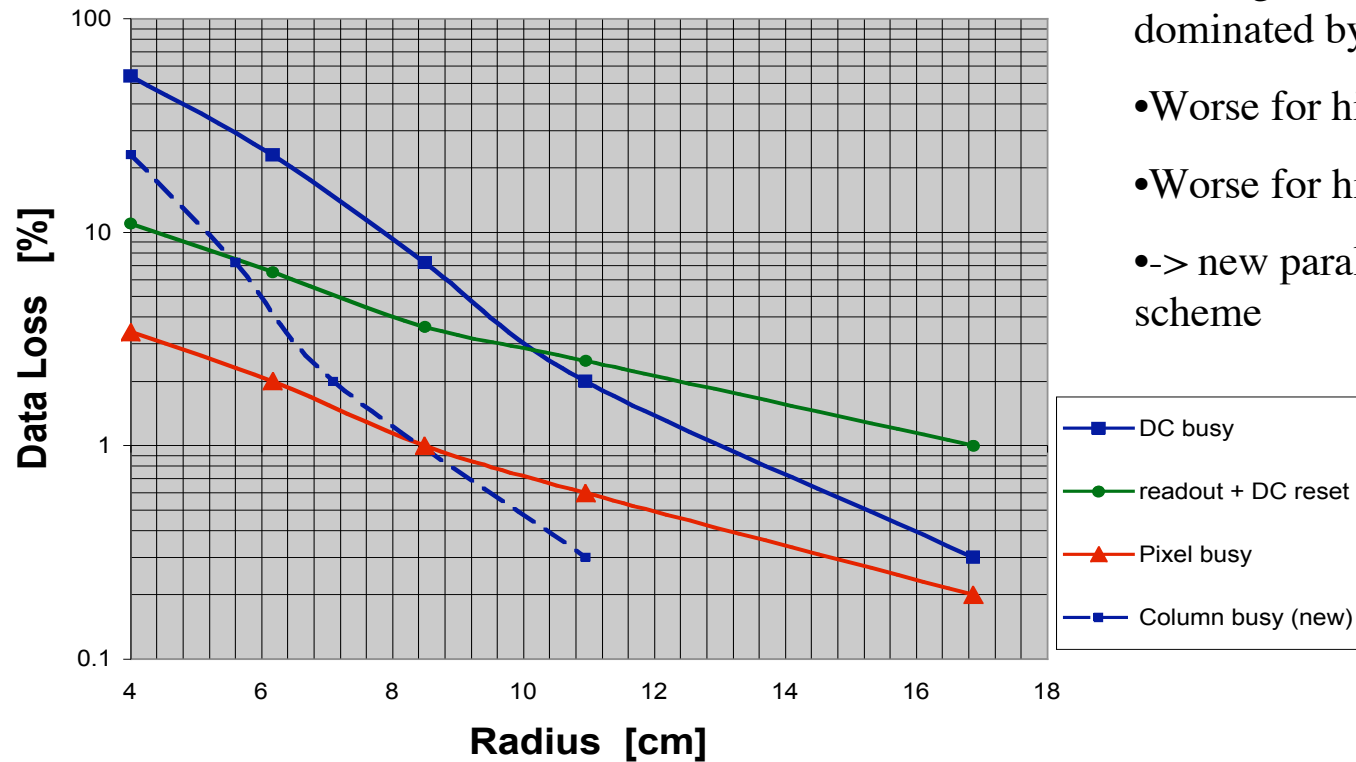•Inefficiency < 7% up to 2.5×10^{34}cm^{-2}s^{-1} (as before)

•In 180nm technology possible:

• column drain per column (instead of double columns)-> dashed line

•Extra buffer stage for L1 validated data waiting for readout->columns are no longer blocked. Negligible readout and reset losses

•5% inefficiency at 5×10^{34}cm^{-2}s^{-1} dominated by busy column drain: no further improvement possible based on this architecture

Legend:
- DC busy
- Readout + DC reset
- Pixel busy
- Column busy (new)

X-axis: Luminosity [10^34]
Y-axis: Data Loss [%]

Inefficiency vs radius for $10 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$

- Cannot operate < 7cm
- For higher radii data loss dominated by readout losses
- Worse for higher L1 trigger rates
- Worse for higher trigger latencies
- -> new parallel module readout scheme

Conclusions

- Expected data loss in present pixel system agrees well with measurements up to very high track rates

- Main source of data loss beyond 10^{34}cm^{-2}s^{-1} are buffer overflows

- Different ‚soft‘ upgrade stages considered:
  – Doubling buffer sizes in present 0.25μm ROCs possible. This allows moderate upgrade up to ~2×10^{34}cm^{-2}s^{-1} @ 4cm (1 month R&D)
  – For higher rates need to go to 180nm technology (1 year R&D)
  – Cannot handle 10xLHC rate @ 4cm. Minimum is r≈7cm or 5×10^{34}cm^{-2}s^{-1} @ 4cm with ineff.<5%

- This assumes the trigger latency stays about the same (3.2μs). If it gets larger, need larger buffers->130nm technology (major R&D project, 2-3 years)