A high performance beam hodoscope for the P326 experiment at CERN

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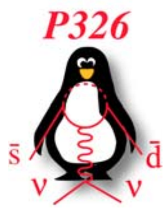
Outline

- **What are P326 and the Gigatracker**
- **The specifications**
- **Timing resolution: can we achieve 200 ps?**
- **General chip architecture, data rate**
- **Radiation effects (chip + detector)**
- **Layout considerations: how to cover the beam area?**
- **Conclusions**



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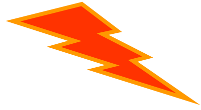

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P326

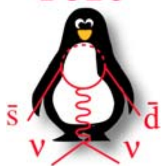
Proposed experiment to measure rare kaon decays at the CERN Super Proton Synchrotron (SPS):

$$K^+ \Rightarrow \pi^+ \nu\bar{\nu}$$

This is a very rare event: the branching ratio is $\sim 10^{-11}$. Many more probable competing events have to be suppressed.

The experiment aims at:

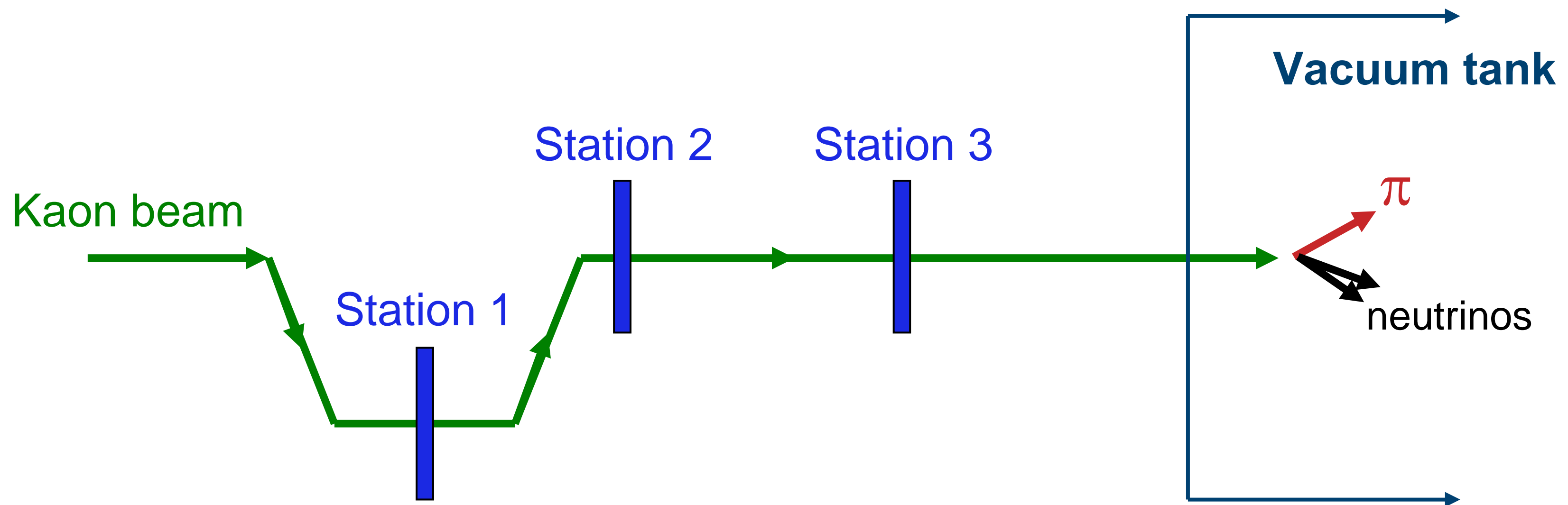
- Collecting ~ 5×10^{12} kaon decays per year
- Collecting ~ 100 events at the SPS by 2010
- Using the NA48 beamline

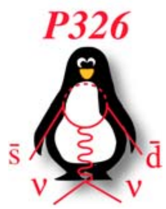


(Last) Experiment Layout

Duties of the Gigatracker

- Provide momentum measurement (stations 1 and 2)
- Tracking of particles up to the decay tank (stations 2 and 3)
- Provide time information to make a tight kaon-pion time coincidence with a fast hodoscope (CHOD) downstream
- Present a minimum disturbance for the beam (low material!)





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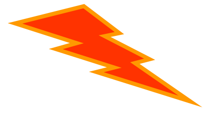

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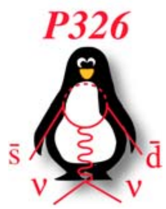
The Gigatracker Specifications

The Gigatracker is an "object" which has to:

- Track 1 billion particle per second
  - High data rate
- Over a surface of ~ 17 cm^2
  - Might be difficult to be covered uniformly with silicon ICs
- With a time resolution on the track of 140 ps (200 ps per station)
  - Very difficult with thin silicon detectors
- With a spatial resolution of 100 μm
  - Not a problem with silicon
- With a minimum material budget (~ 0.4 % X_0 per station)
  - Very difficult
- In vacuum and in a harsh radiation environment
  - I know more pleasant environments, especially for the detector

Can we meet the specifications using the Hybrid Pixel Detector Technology?



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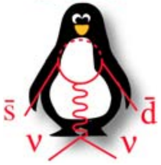
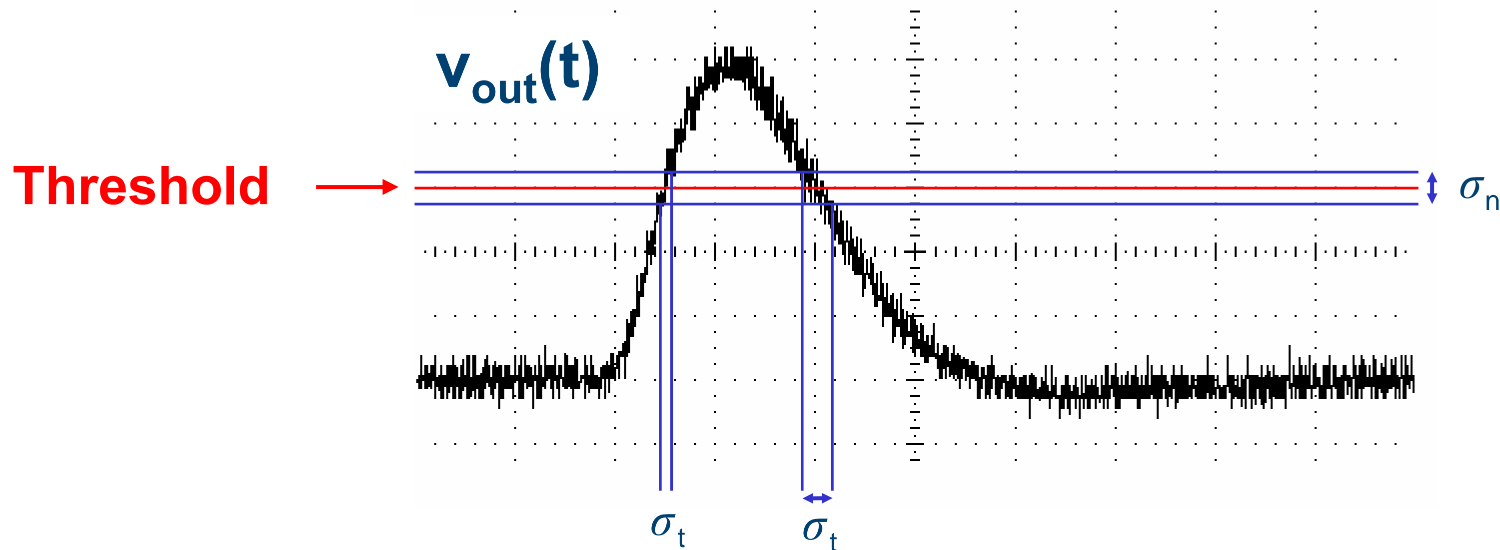


The timing resolution

The best achievable timing resolution σ_t depends on:

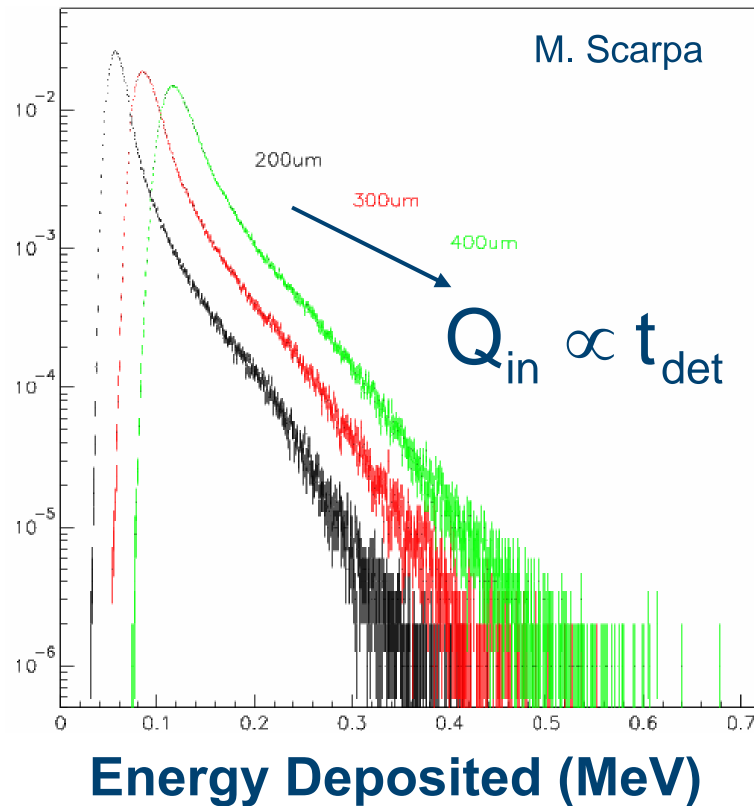
- **Electronic noise (σ_{n_out})**
- **Signal slope**
  - **Signal amplitude**
  - **Signal speed**

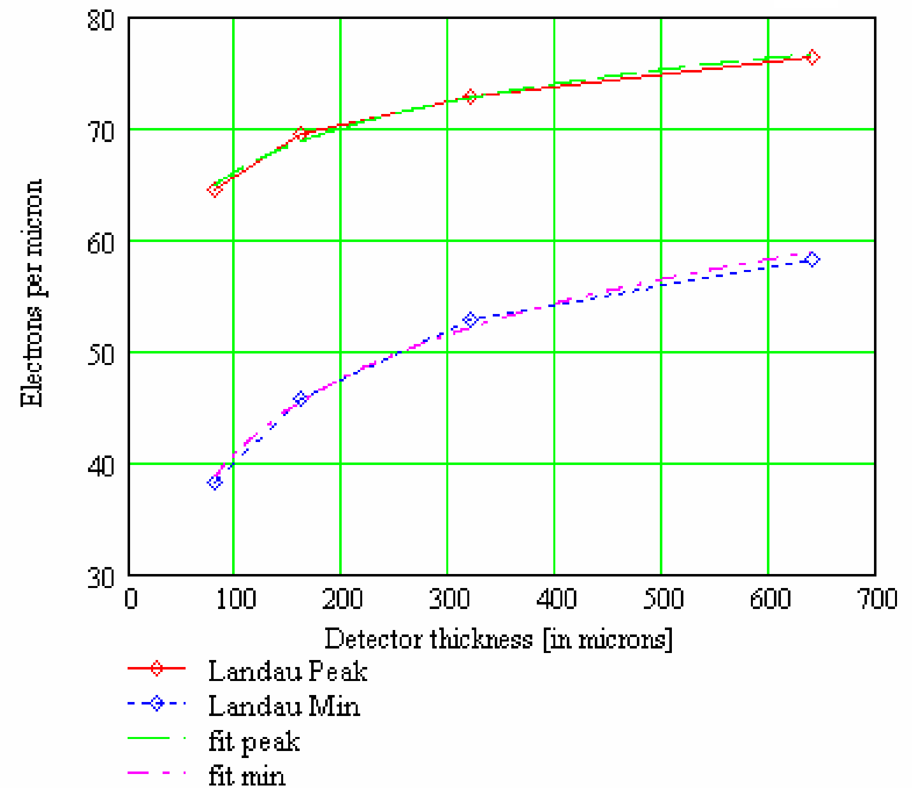
$$\sigma_t = \frac{\sigma_{n_out}}{\frac{dv_{out}(t)}{dt}}$$

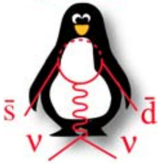


Silicon detector signal amplitude

The amount of charge deposited follows the Landau distribution. Thicker detectors give more signal!

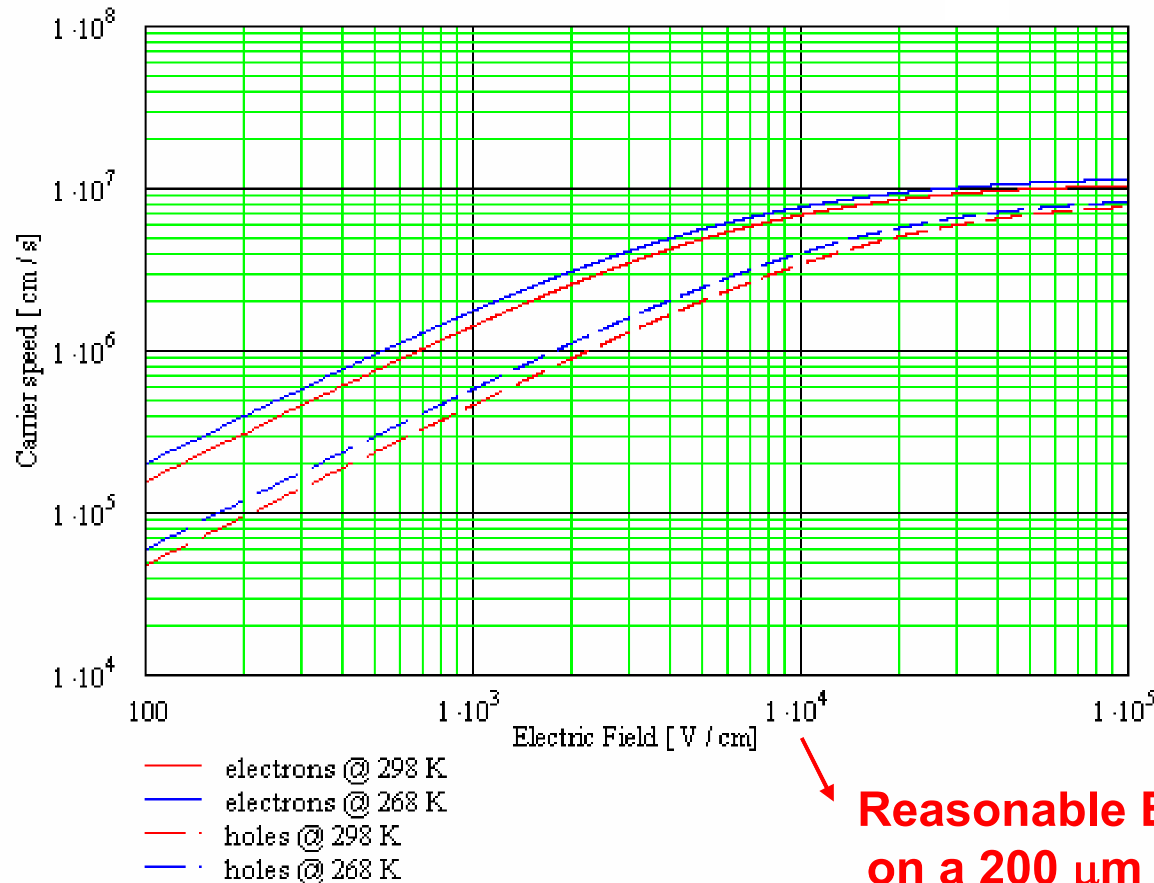




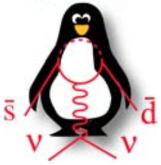


Silicon detector speed

The carrier speed depends on the carrier type, on the applied bias voltage and on the detector temperature



Reasonable E field: ~ 200 V on a 200 μm thick detector



Silicon detector speed (2)

Signal shape example: we assume an over depleted detector

$E = 10^4$ V/cm

Current [A]

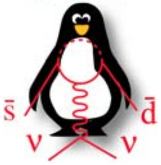
$4 \cdot 10^{-7}$
$3 \cdot 10^{-7}$
$2 \cdot 10^{-7}$
$1 \cdot 10^{-7}$
0

0 2 4 6 8 10

Time [ns]

electrons
holes
total

All the created electrons and holes are collected



Silicon detector speed (3)

If we want to collect all the charge (not to loose signal) we do have to make the electronics slower than the detector

E = 10^4 V/cm

Hole collection time [ns]

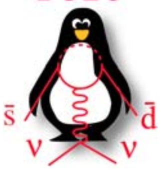
20
15
10
5
0

100 200 300 400 500 600

Detector thickness [um]

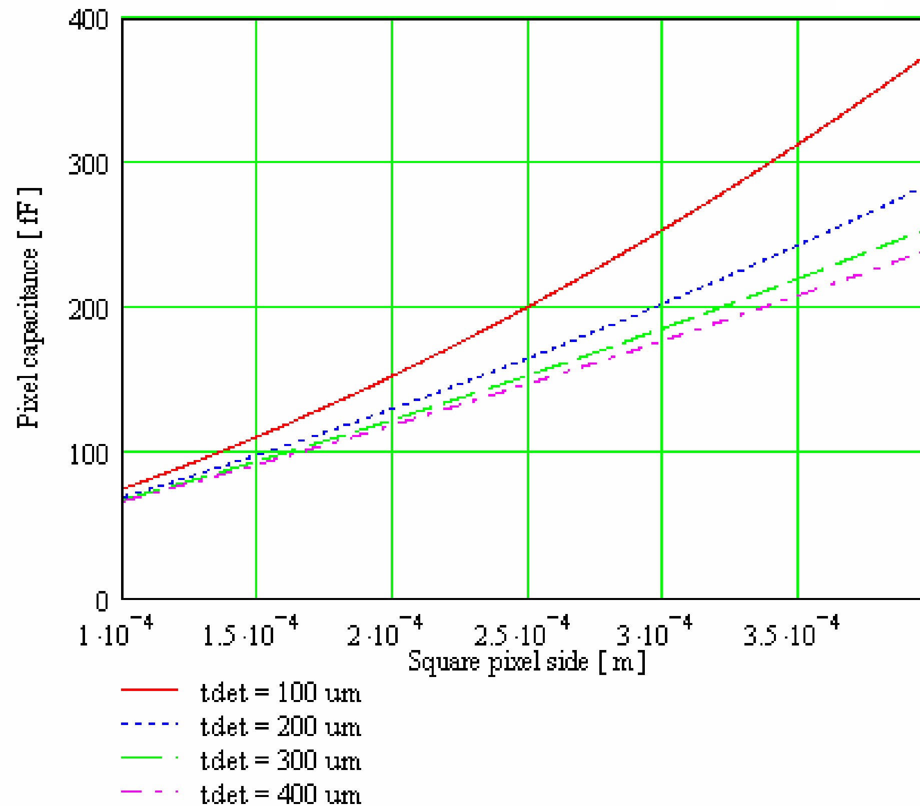
298 K
268 K

$$\tau_{coll_h} = \frac{t_{det}}{v_h(E, T_{det})}$$

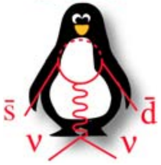


Detector capacitance

The detector capacitance is a function of the detector thickness t_{det} and of the pixel size. The capacitance of each pixel (C_{det}) has a component dependent on the pixel area and one on the pixel perimeter. The latter is normally quite important and has a very little dependence on t_{det}.

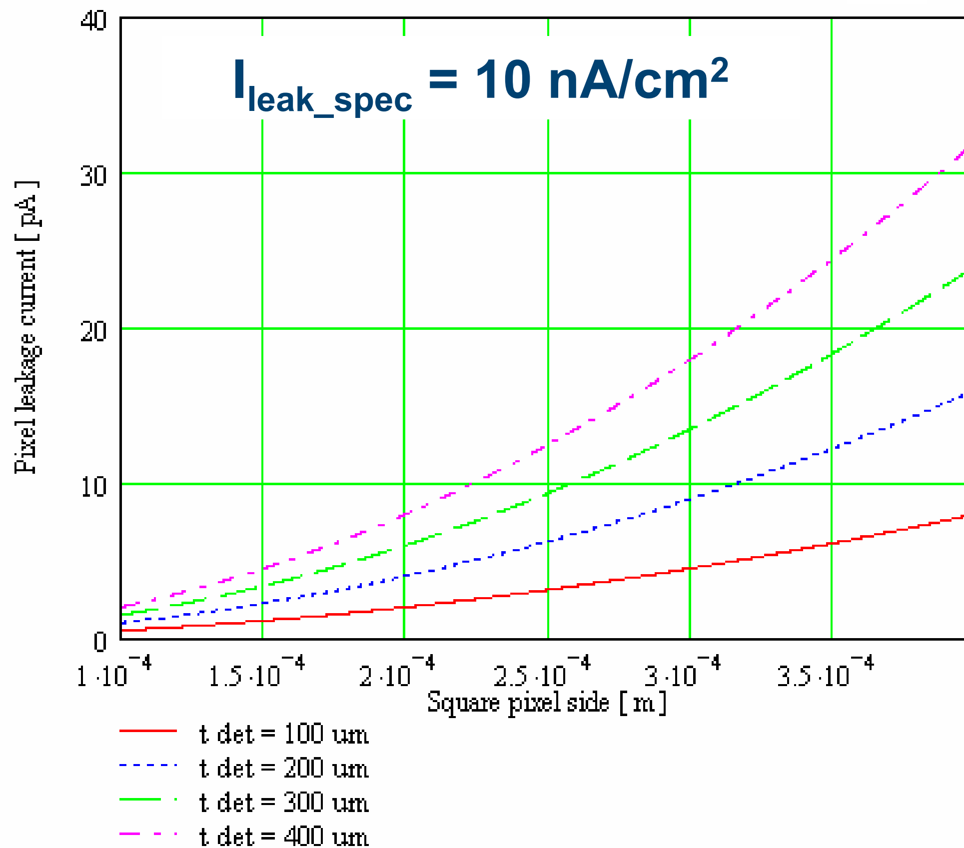


$$C_{det} \propto \frac{\text{pixel size}}{t_{det}}$$



Detector leakage current

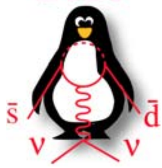
If the dominating component of the leakage current comes from the bulk (as it should be), the leakage current of each pixel I_{leak} varies linearly with the volume of the pixel.



$$I_{leak} \propto (\text{pixel size}) \cdot t_{det}$$

Some assumptions

- **Electric field in the detector: 10^4 V/cm**
- **Max power dissipation allowed: 1.2 W/cm^2**
- **Only 30% of the power per pixel goes into the input transistor**
- **Minimum signal: Minimum of the Landau divided by 2 to take into account the charge sharing**
- **Technology considered: IBM 0.25 μm and IBM 0.13 μm CMOS (similar results obtained)**
- **All the calculations done in the following take into account the variations of C_{gs} and g_m depending on the transistor working region**
- **We always chose the shaping time equal to the hole collection time (this for the best timing resolution)**

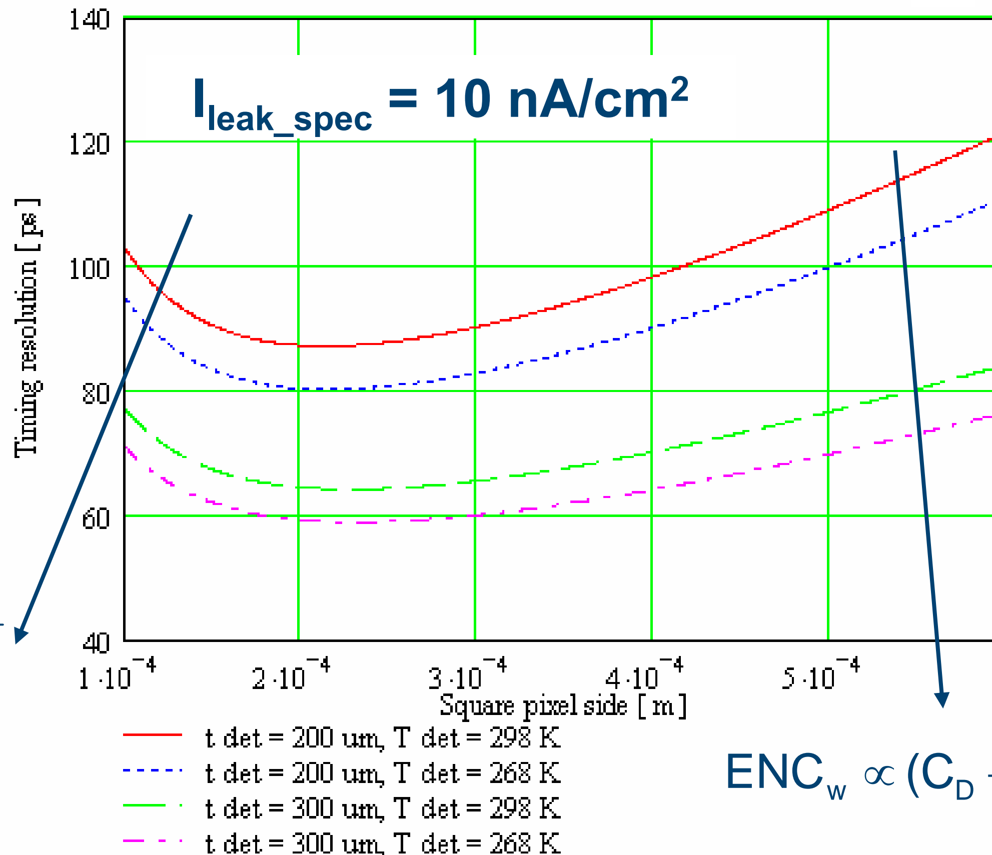


Optimum pixel size

Before irradiation the leakage current is normally very low, and at short shaping times the noise is dominated by the white noise components.

$$\sigma_t = \frac{ENC \cdot \tau_p}{Q_{in}}$$

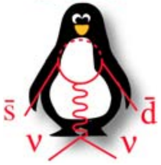
The shaping time is here chosen equal to the hole collection time (to go fast without loosing signal)



$$ENC_w \propto \sqrt{kT\gamma \frac{1}{g_m} \frac{1}{\tau_p}}$$

$$I_{DS} = \frac{1}{\text{pixel size}}$$

$$ENC_w \propto (C_D + C_{gs})$$



Noise vs shaping time (low I_{leak})

I_{leak} = 10 pA, C_{det} = 200 fF, I_{DS} = 130 μA

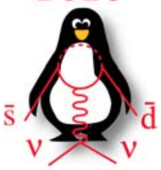
Noise [electrons]

200
150
100
50
0

$1 \cdot 10^{-9}$ $1 \cdot 10^{-8}$ $1 \cdot 10^{-7}$ $1 \cdot 10^{-6}$

Shaping time [s]

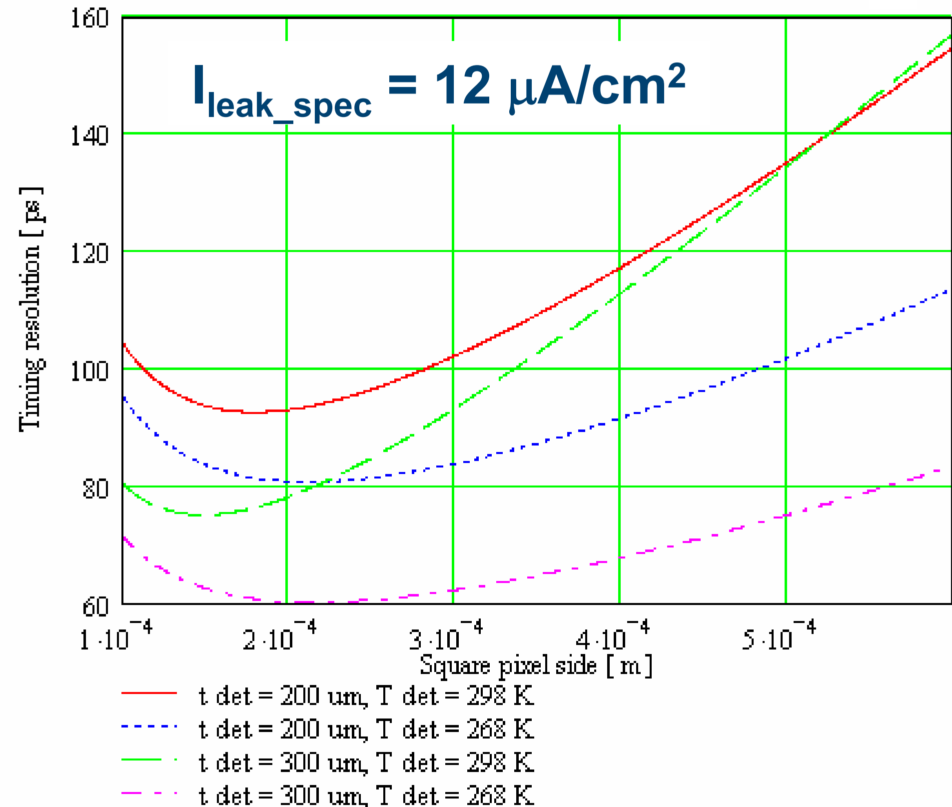
ENC 1/f
ENC w
ENC p
ENC



Optimum pixel size (2)

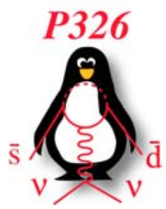
For higher leakage currents (after irradiation) the parallel noise component (ENC_p) become also very important, as we can see in the plots at room temperature.

Only cooling down we go (almost) back to the case in which the noise is dominated by the white noise.



Conclusion: 300 μm by 300 μm pixel size seems a good choice. It is close to the optimum and it gives the necessary spatial resolution. But we have to cool down the detector after irradiation!

Conclusion 2: very small pixels not the best (for a constant power budget)!



Noise vs shaping time (high I_{leak})

I_{leak} = 10 nA, C_{det} = 200 fF, I_{DS} = 130 μA

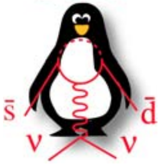
Noise [electrons]

500
400
300
200
100
0

$1 \cdot 10^{-9}$ $1 \cdot 10^{-8}$ $1 \cdot 10^{-7}$ $1 \cdot 10^{-6}$

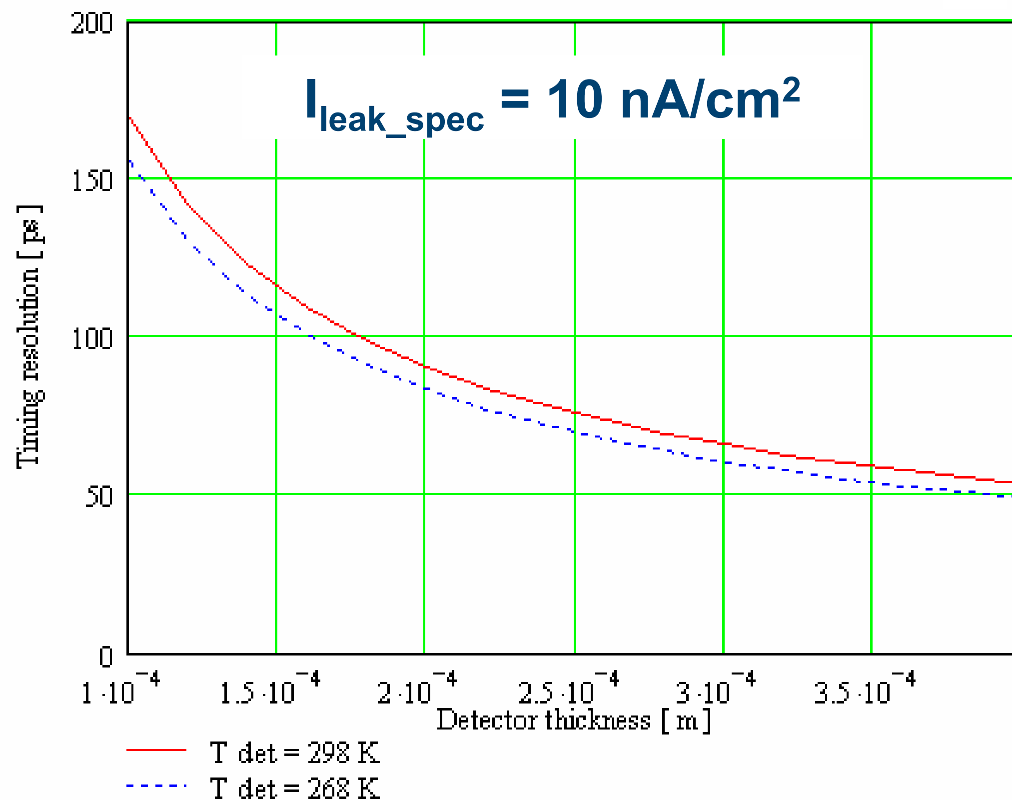
Shaping time [s]

ENC 1/f
ENC w
ENC p
ENC



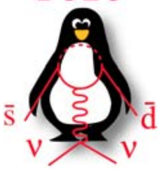
Optimum detector thickness

For low leakage currents we are dominated by white noise, which decreases increasing the shaping time



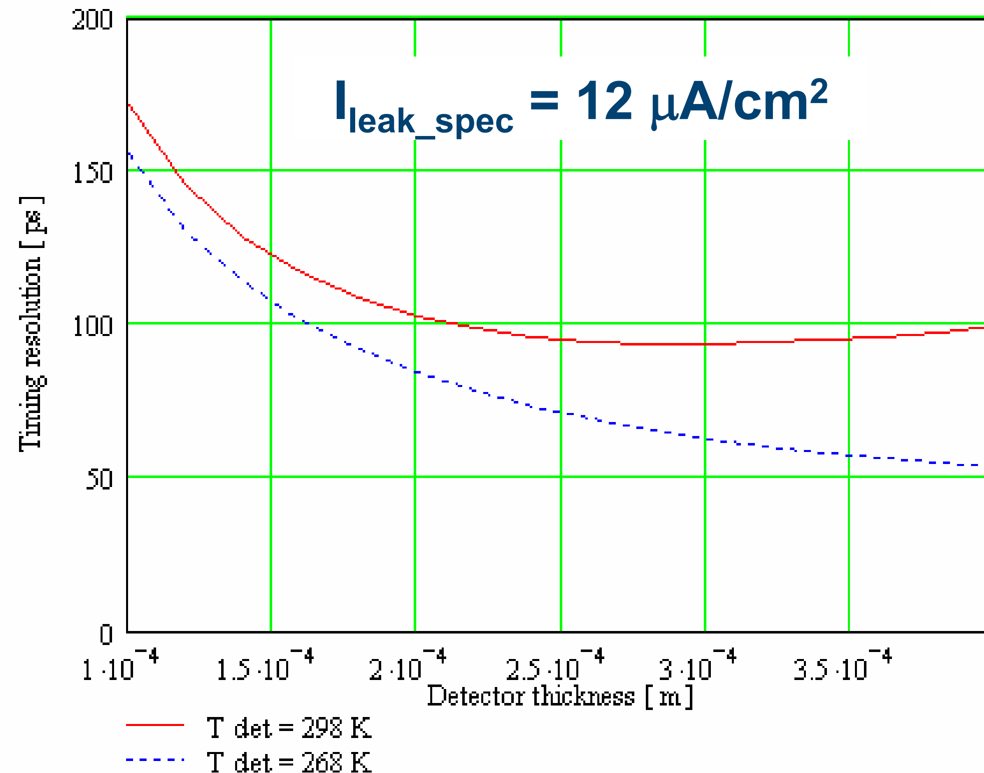
$$\sigma_t = \frac{ENC \cdot \tau_p}{Q_{in}}$$

τ_p increases linearly with the detector thickness, Q_{in} almost linearly.

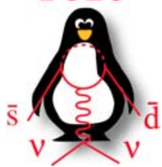


Optimum detector thickness (2)

For high leakage currents (like for an irradiated detector at room temperature) increasing the shaping time does not decrease the noise anymore!

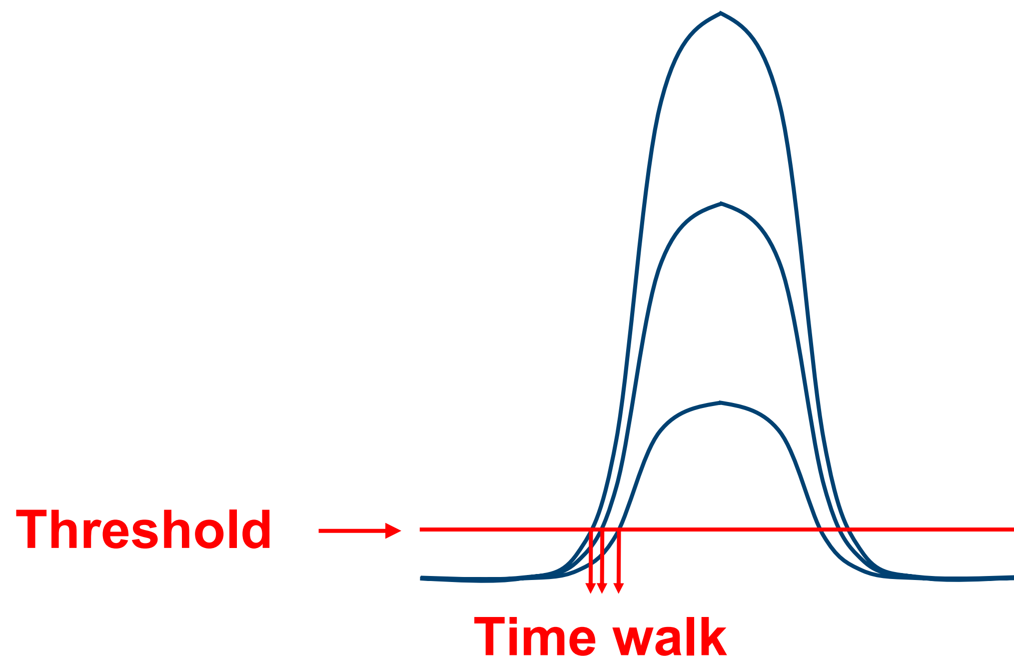


Conclusion: **a 200 μm thick detector is a good choice. This gives the required timing resolution (also after irradiation) and low material budget. A cooled thicker detector would be better from the timing resolution point of view.**



The time walk

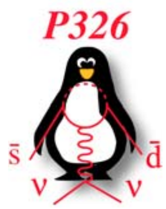
Signals with same shape but different amplitude will cross the threshold at different times. This spread can easily be a few nanoseconds.



We are investigating several ways to compensate for this:

- **Zero crossing or constant fraction discriminators**
- **Time over threshold techniques**

This is clearly a key issue which has to be solved!



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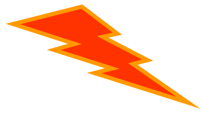

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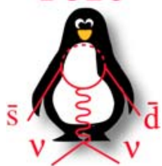
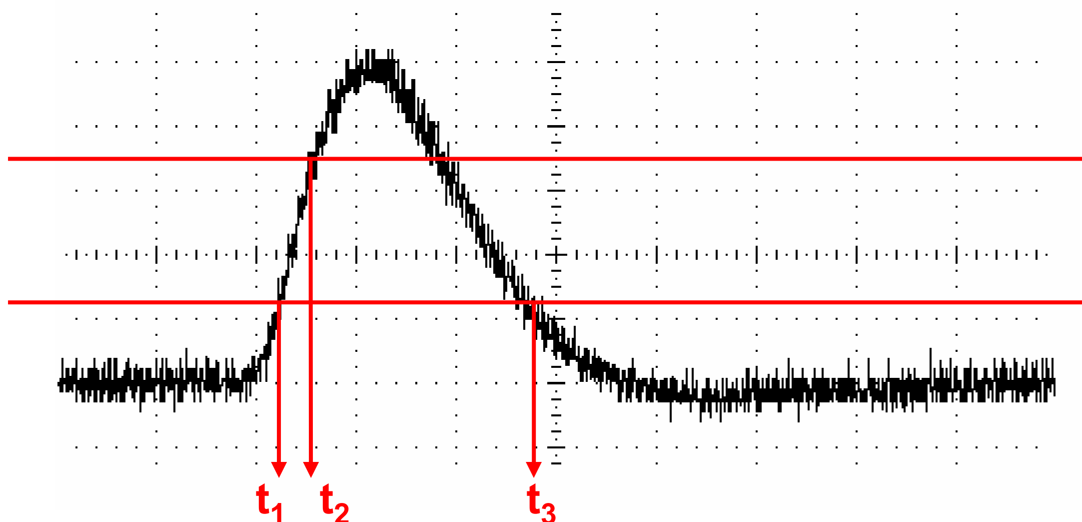
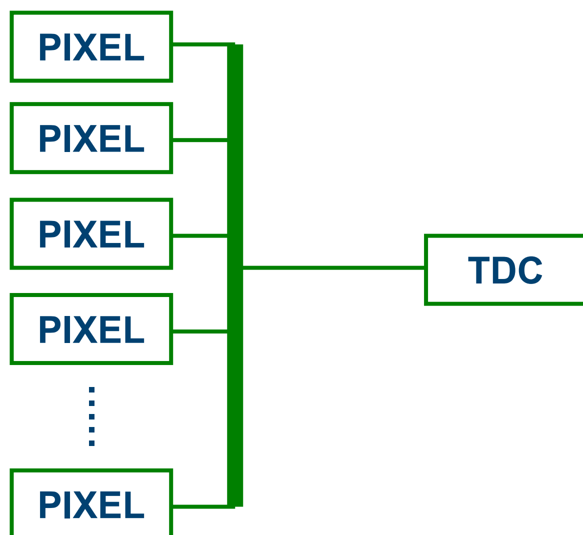


And after the discriminator what?

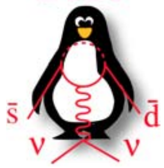


To compensate for the time walk one can use t_1 and t_3 (TOT). t_1 and t_2 is even better, because the slope of t_2 is bigger and we keep the "bus" busy for a shorter time (important for the efficiency).



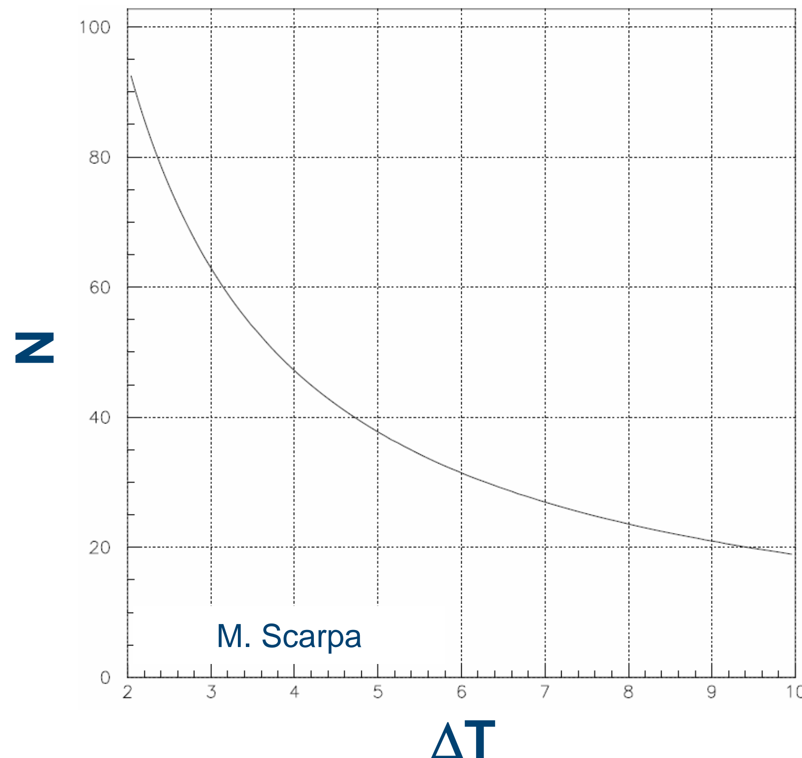
To measure the time one possibility is to use a Time-to-Digital Converter (TDC) per group of pixels.

How many pixels can we connect to the same TDC for a given efficiency?



TDC Inefficiency

For 1 GHz total rate, 300 μm by 300 μm pixels and a beam area of 36 mm by 48 mm the average rate per pixel is 52 kHz. The probability of having two pixels (connected to the same TDC) hit in a time interval ΔT depends on the total number of pixels N going to the same TDC.
For a 1% inefficiency and an average rate of 52 kHz we have:



Data rate

Let's assume a matrix of 32 columns and 60 rows (9.6 mm by 18 mm)

How many bits per hit?

t_1 7 bits (10 ns / 128 = 78 ps)
t_2 7 bits
Longer time 7 bits (10 ns * 128 = 1.28 μs)
Pixel address 11 bits

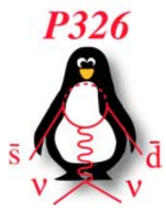
} **32 bits per hit**

What is the data rate per chip?

The average rate per chip is ~ 100 MHz
100 MHz * 32 bits gives 3.2 Gbit/s!!!

Transmitting this amount of data in principle should not be a big problem. But how well can a Gbit/s transmitter coexist on the chip together with all the rest? Is substrate noise an issue?

We are working on test structures to better understand this (possible) problem.



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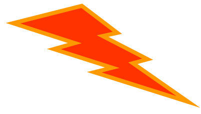

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- Layout considerations: how to cover the beam area?
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Radiation-hard circuits

Using a CMOS technology we have to worry "only" about TID effects and SEEs

- In the Microelectronics Group at CERN we have developed layout techniques which allow solving the most disturbing TID effects and the Single Event Latch-up (SEL) issue

- Single Event Gate Rapture (SEGR) never occurs in advanced CMOS processes

- Single Event Upset (SEU) still remains an issue. We will have to protect the most critical digital blocks against it (special circuit architecture, redundancy, …)

Radiation-hard detectors (?)

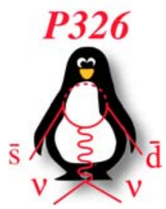
This is a serious problem.

The flux integrated over 100 working days is:

- **Average: $2.7 \cdot 10^{13}$ 1 MeV neutrons/cm^2**
- **Center: $8.9 \cdot 10^{13}$ 1 MeV neutrons/cm^2**

We need a low leakage current and, for speed, we need to operate the detector well over depleted.

It will therefore be mandatory to operate the detector at low temperatures, and we might need to change the stations from time to time.



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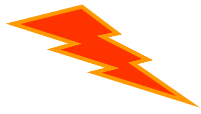

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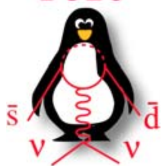


Best option for min material budget

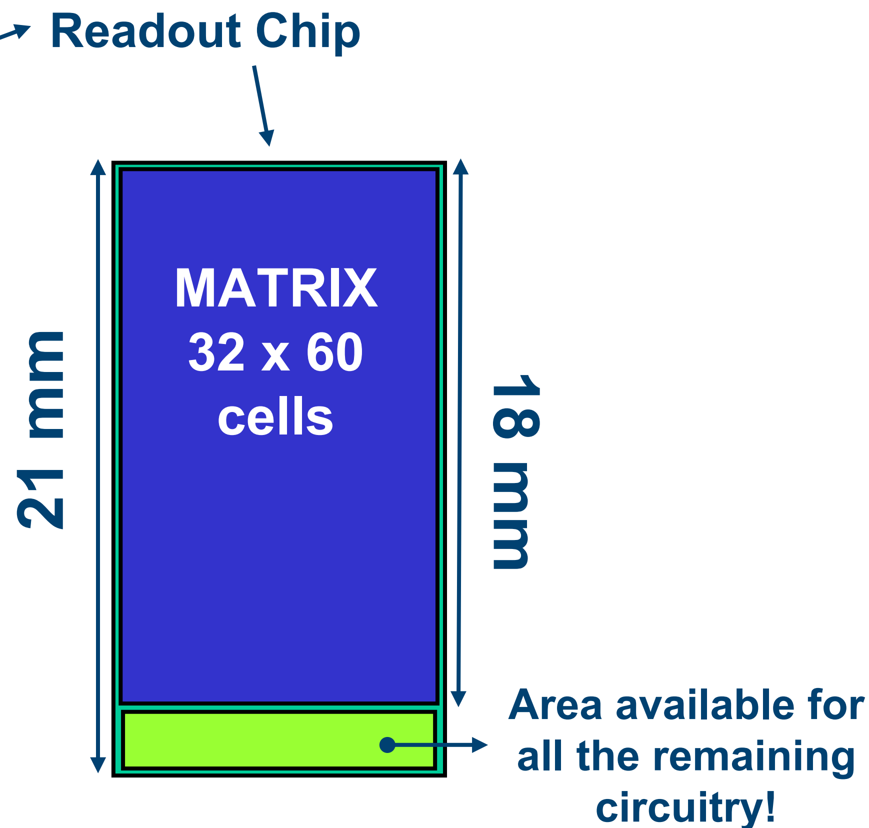
48 mm

36 mm

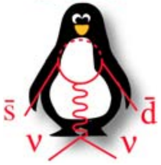
Detector

Support (Carbon Fiber?)

BUS (VDD, GND, Signals)



PROBLEM:
POWER DISTRIBUTION FOR THE MATRIX, CHIP SIZE



Intermediate option

18 mm

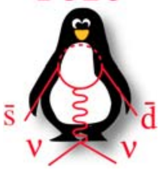
48 mm

21 mm

MATRIX
32 x 60
cells

18 mm

In this case the problem of the power distribution is reduced but we still have a very small area for all the rest of the circuits, a very long chip and we have a non uniform material budget in the centre of the beam!



Possible best overall choice?

12 mm

48 mm

18 mm

MATRIX
32 x 40
cells

12 mm

This solution still has non uniformities in the material budget (but not in the beam centre). On the other hand it gives:

- **Power distribution on two sides of the chip**
- **More area for the circuits not in the matrix**
- **A smaller chip (better yield, lower cost)**

Conclusions

- **The specifications have been discussed in detail and are now quite clear (but more simulations are needed on the material budget issue)**
- **The most difficult issues to be solved are:**
  - **The timing resolution (time walk)**
  - **The high data rate**
  - **The chip size (power distribution, non uniformities…)**
  - **Cooling**
  - **Detector radiation hardness**

The project looks very challenging but…
FEASIBLE!

SPARE SLIDES

Electronic Noise

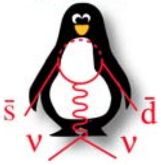
The signal from the detector will be amplified by a charge amplifier.

The noise deteriorating the time resolution is mainly due to the noise of the amplifier input transistor and to the detector leakage current shot noise (parallel noise).

In CMOS technologies, the transistors have mainly two noise components:

1. **Channel thermal noise (white noise)**
2. **1/f noise**

In the following, we will express the noise at the input of the amplifier as an Equivalent Noise Charge (ENC)



Electronic Noise (2)

C_F

$$V_{out_MAX} = G \cdot Q_{in}$$

N.B. This holds if $\tau_p > \tau_{coll_holes}$

$$Q_{in} = \int i_{in}(t)dt$$

$i_{in}(t)$

C_D

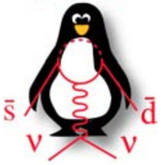
SHAPER

$v_{out}(t)$

V_{out_MAX}

τ_p

$$\sigma_t = \frac{\sigma_{n_out}}{\frac{dv_{out}(t)}{dt}} = \frac{ENC \cdot G}{\frac{V_{out_MAX}}{\tau_p}} = \frac{ENC \cdot G \cdot \tau_p}{Q_{in} \cdot G} = \frac{ENC \cdot \tau_p}{Q_{in}}$$



Electronic Noise (3)

$$\overline{v_n^2} = 4kT\gamma \frac{1}{g_m} + \frac{K_f}{C_{ox}WL}\frac{1}{f}$$

$$g_m = f(I_{DS}, W, L)$$

$$C_{gs} = f(I_{DS}, W, L)$$

C_F

$\overline{v_n^2}$ I_{DS} C_{gs}

SHAPER τ_p

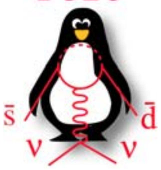
$i_{in}(t)$ + I_{leak} C_D $\overline{i_n^2} = 2qI_{leak}$

$$ENC_{1/f} \propto (C_D + C_{gs})\sqrt{\frac{K_f}{C_{ox}WL}}$$

$$ENC_w \propto (C_D + C_{gs})\sqrt{kT\gamma \frac{1}{g_m}\frac{1}{\tau_p}}$$

$$ENC = \sqrt{ENC_w^2 + ENC_p^2 + ENC_{1/f}^2}$$

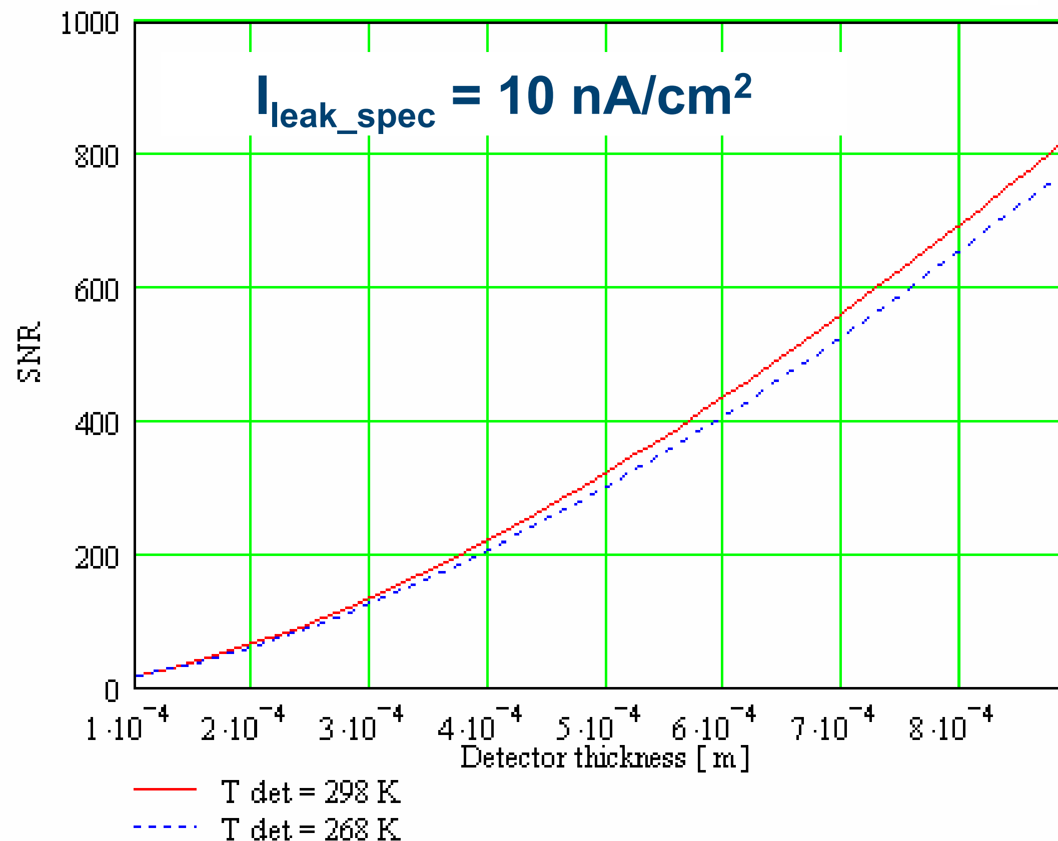
$$ENC_p \propto \sqrt{2qI_{leak}\tau_p}$$

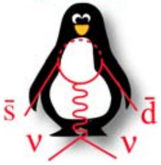


Signal to Noise Ratio (SNR)

The requirement on low noise given by the timing resolution normally gives a very good SNR. Increasing the detector thickness we increase the input signal and decrease the noise (if the white noise is dominant).

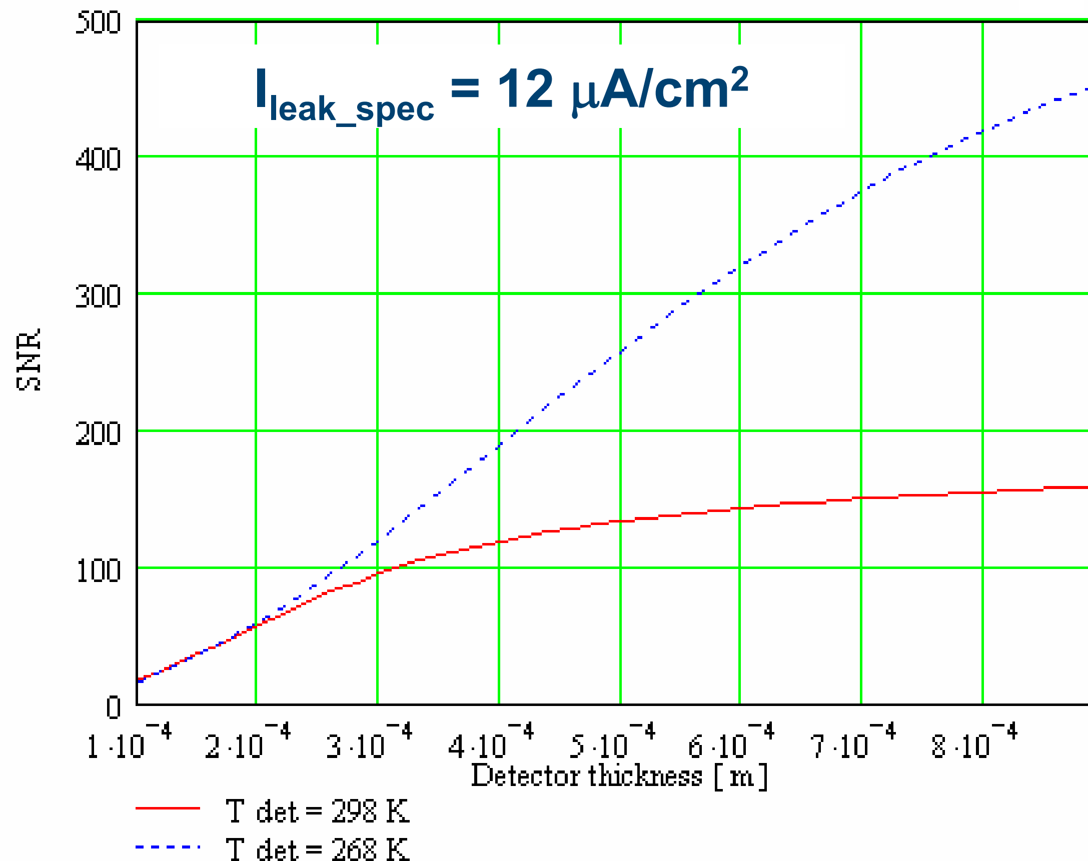
$$SNR = \frac{Q_{in}}{ENC}$$





Signal to Noise Ratio (2)

When the parallel noise (from the leakage current) becomes also important, the SNR still increases for thicker detectors (the input signal increases), but at a slower pace (the noise decreases less or increases).

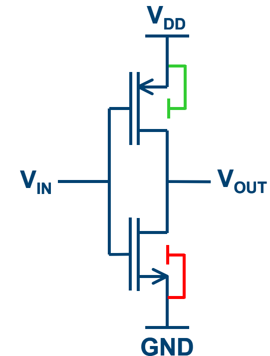


Digital noise in mixed-signal ICs

Integrating analog blocks on the same chip with digital circuits can have some serious implications on the overall performance of the circuit, due to the influence of the "noisy" digital part on the "sensitive" analog part of the chip.

The switching noise originated from the digital circuits can be coupled in the analog part through:

- **The power and ground lines**
- **The parasitic capacitances between interconnection lines**
- **The common substrate**



The substrate noise problem is the most difficult to solve.

Noise reduction techniques

- Quiet the Talker. Examples (if at all possible !!!):
  - ➢ Avoid switching large transient supply current
  - ➢ Reduce chip I/O driver generated noise
  - ➢ Maximize number of chip power pads and use on-chip decoupling
- Isolate the Listener. Examples:
  - ➢ Use on-chip shielding
  - ➢ Separate chip power connections for noisy and sensitive circuits
  - ➢ Other techniques depend on the type of substrate. See next slide
- Close the Listener's ears. Examples:
  - ➢ Design for high CMRR and PSRR
  - ➢ Use minimum required bandwidth
  - ➢ Use differential circuit architectures
  - ➢ Pay a lot of attention to the layout

Different types of substrates

There are mainly two types of wafers:

1. **Lightly doped wafers: “high” resistivity, in the order of 10 Ω-cm.**

2. **Heavily doped wafers: usually made up by a “low” resitivity bulk (~ 10 mΩ/cm) with a “high” resistivity epitaxial layer on top.**

TSMC, UMC, IBM and STM (below 180 nm) offer type 1

Substrate noise: how to reduce it

To minimize the impact of disturbances coming from the substrate on the sensitive analog blocks, we have mainly three ways:

- **Separate the "noisy" blocks from the "quiet" blocks. This is effective especially in uniform lightly doped substrates. For heavily doped substrates, it is useless to use a separation greater that about 4 times the epitaxial layer thickness.**
- **In n-well processes, p+ guard rings can be used around the different blocks. Unfortunately, this is again effective mainly for lightly doped substrates. Guard rings (both analog and digital) should be biased with separate pins.**
- **The most effective way to reduce substrate noise is to ground the substrate itself in the most "solid" possible way (no inductance between the substrate and ground). This can be done using many ground pins to reduce the inductance, or, even better, having a good contact on the back of the chip (metallization) and gluing the chip with a conductive glue on a solid ground plane.**
- **Separate the ground contact from the substrate contact in the digital logic cells, to avoid to inject the digital switching current directly into the substrate.**

Interaction radiation - ICs

The two most important phenomena to be considered are ionization and nuclear displacement.

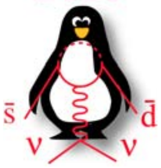
Neutrons give origin mainly to nuclear displacement.

Photons give ionization.

Charged hadrons and heavy ions give both at the same time.

For ionization we talk about Total Ionizing Dose (TID), for nuclear displacement about Fluence

In our case the beam will be made of
π^+ (60%), p (20%), e^+ (14%), K^+ (6%)



Interaction radiation – ICs (2)

Cumulative Effects
- **TID**
  - **MOS**
  - **Bipolars**
- **Displacement**
  - **Bipolars**
  - **Optoelectronics**

Single Event Effects (SEE)
- **Non Catastrophic (SEU)** → **MOS**
- **Catastrophic (SEGR, SEL)** → **MOS**