Front-end Electronics for Silicon Trackers readout Deep Sub-Micron Technology

The case of Silicon strips at the ILC

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and

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Outline

- Context of the Silicon strips for the ILC
- Integrated electronics
- 180nm CMOS chip
- First design in 130nm
- Future plans

Silicon strips for the ILC

Silicon strips tracker at the ILC

- a few 10^6 Silicon strips
- 10 - 60 cm long
- Thickness: 200–500µm
- Strip pitch 50–200 µm
- Single sided, AC coupled

Readout parameters

- Interstrip capacitance > 1 pF/cm
  Strip to substrate capacitance > 0.1 pF/cm
- Occupancy defined as % channels hit per BC:

  Outer barrel and end caps layers: < 1 %
  Inner barrel and end caps layers: < a few %
- ILC timing: 1 ms: ~ 3-6000 trains @150-300ns / BC
  100ms in between

Detector data

- Pulse height: Cluster centroid to get position resolution to a few μm

  Detector pulse sampling

- Time: Two scales:

  - Coarse 150-300ns BCO tagging

  Two shaping time ranges 500 ns and 2 μs

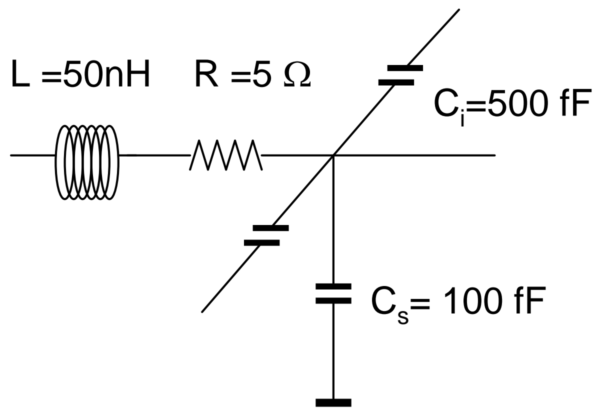
  - Nanosecond timing for the coordinate along the strip

  Not to replace another layer or double sided
  Spatial estimation to a few cm

  Shaping times: 20-100ns

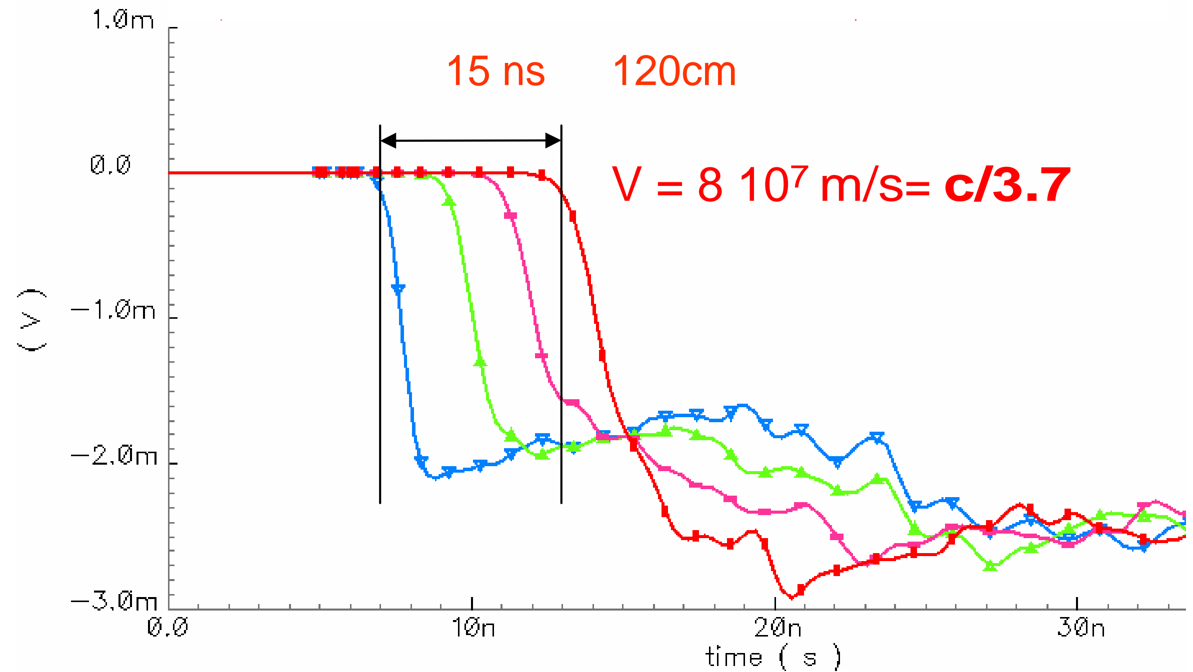
Coordinate along the strip

SPICE



$$V = 1/\sqrt{LC}$$

$$V = 6.3e7\ 10^7\ m/s = \boldsymbol{c/4.7}$$



1 ns time resolution is 8 cm

Integrated Electronics

Integrated Electronics

- **SLAC**

  Calorimetry and tracking

  Charge: linear 1 or 2-gains, 2500 MIPS
  Shaping: reset-sample (2-correlated sampling like)
  Time: BC id

- **UC Santa Cruz**

  Tracking

  Charge: Time Over Threshold, Lo+Hi thresholds, 128 MIPS
  Shaping: µs
  Time: BC id

- **LPNHE Paris**

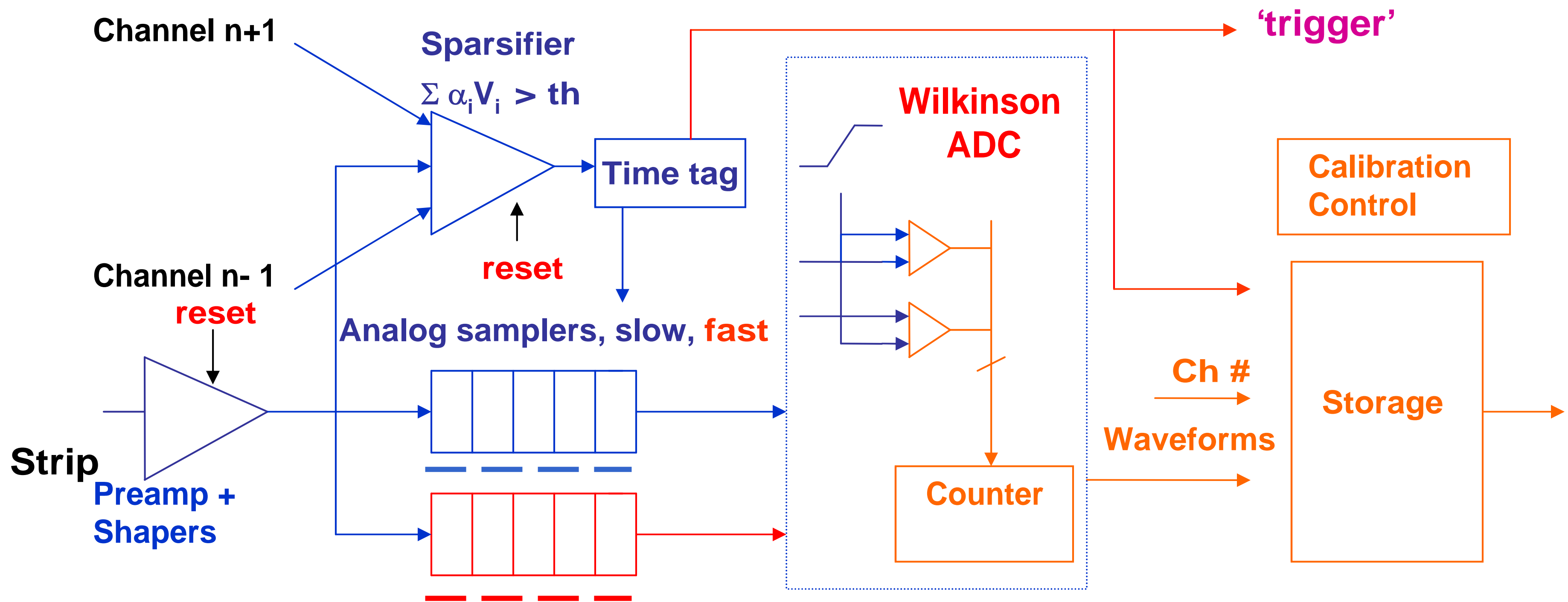
  Tracking

  Charge: linear, multiple sampling including pedestal, 50 MIPS
  Time: 2-scales
  BC id
  ns timing (long. coordinate over strips)

Foreseen on-detector FE chip

- Pulse sampling: 16 samples over 2 shaping times (inc pedestal)
  16-deep sampling analog buffer
- Buffering: a few 10 events buffer
  2D structure: (a few 10)*16 caps/channel
- Sparsification/calibration : On FE chip
- Analog-Digital conversion: Wilkinson optimum (power)
- Digital processing: Amplitude and time estimation + charge cluster algorithm, lossless data compression
- Power: 1/100 ILC duty cycle: FE Power cycling

Foreseen Front-end architecture



Charge 1- 40 MIP, S/N~ 15- 20, Time resolution: BC tagging, fine: ~ 2ns

Technologies: Deep Sub-Micron CMOS 180-130nm
Future: SiGe &/or deeper DSM

Charge measurements

- Preamp + Shaper
  Gain: 20mV/MIP over 1-30 MIP
  S/N = 30 750 e- ENC at 3 µs peaking time
  Reset transistor

- Analog sampler and event buffer
  2D: 16-deep sampling, a few 10-deep events

- Sparsifier
  Threshold an analog sum of 3 adjacent channels
  after pulse shaping. Auto-zeroed.

- ADC
  8-10 bits
  Clocked at 12 MHz, time interpolated if needed

Time measurements

- Time stamping

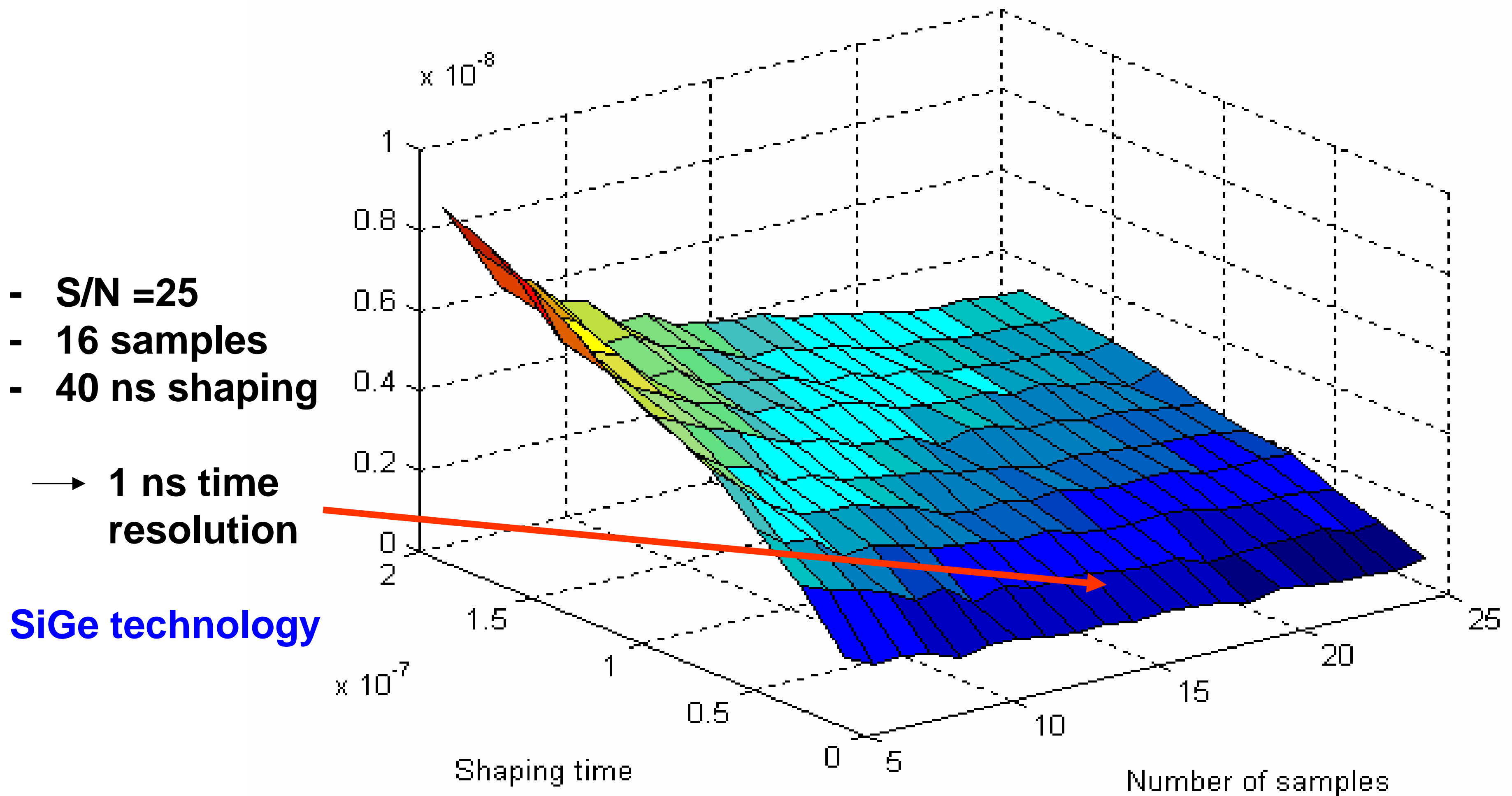
  BC tagging: resolution of 30 to 50 ns
  Time-stamp the sparsifier output at 4 * BCO clock (83 ns)

- Fine time measurement

  Order of 1 ns
  32 * BCO clock (12ns on-chip vernier sampling clock)
  Use digital signal processing over 16 digitized samples

Expected time resolution

Simulated time resolution using multiple sampling and a least square fit of the shaper pulse algorithm (Bill Cleland)



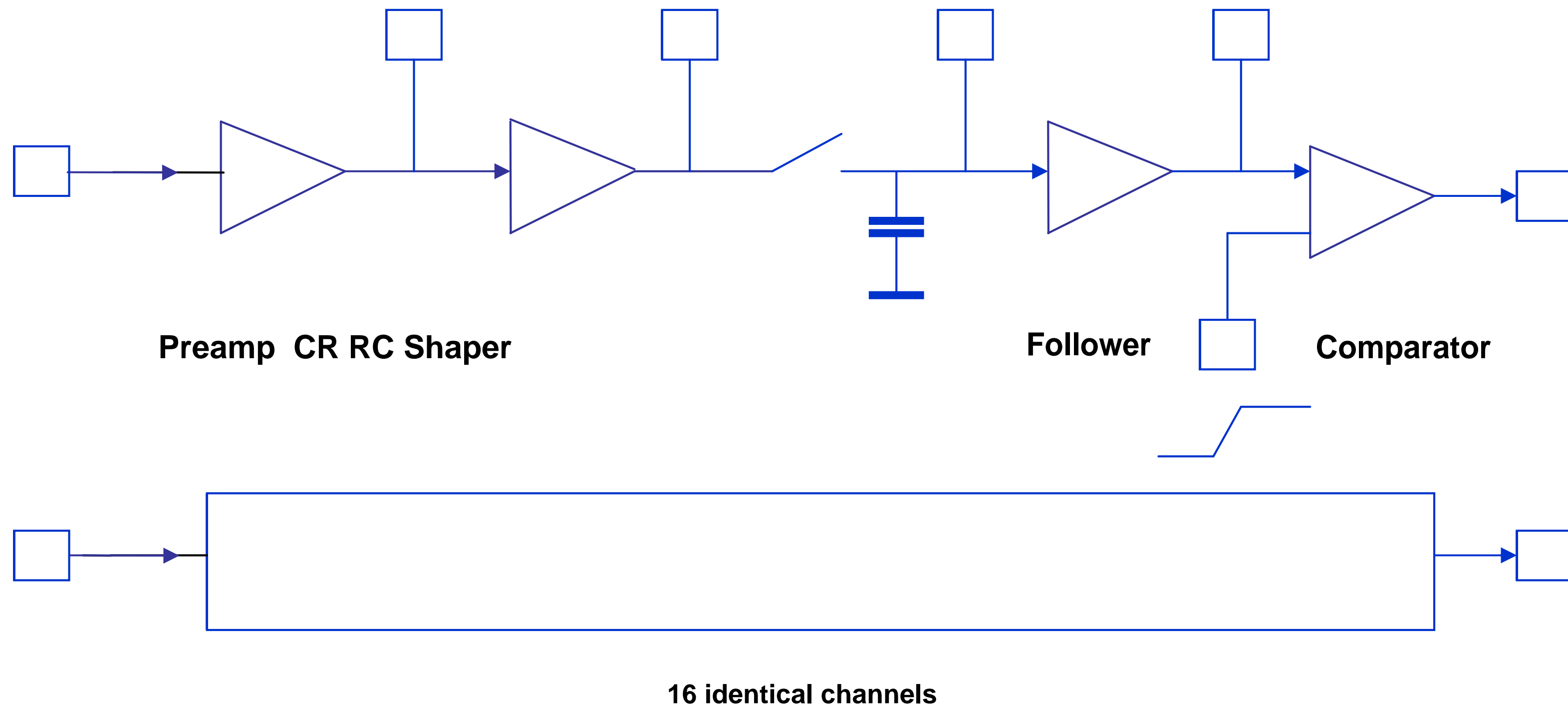
CMOS 180nm Chip

UMC CMOS 180nm technology

180 nm Mixed-mode process

- 6 metals layers
- 3.3 V transistor
- Cox = 0.0049 F/m²
- Metal/Metal capacitance = 1fF/mm²
- Gate's minimum width= 0.5mm
- Various V_t options

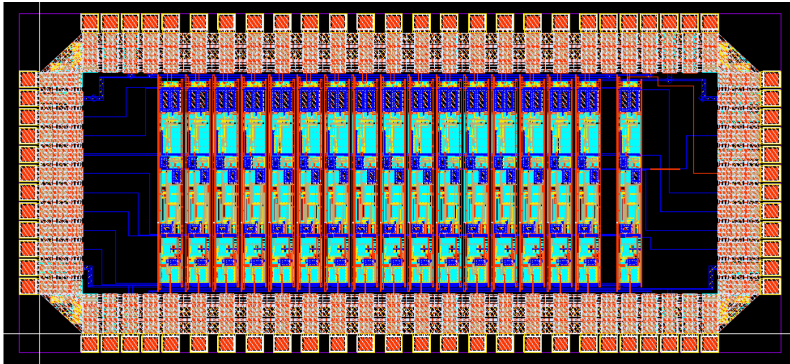
Front-end test chip in CMOS 180nm

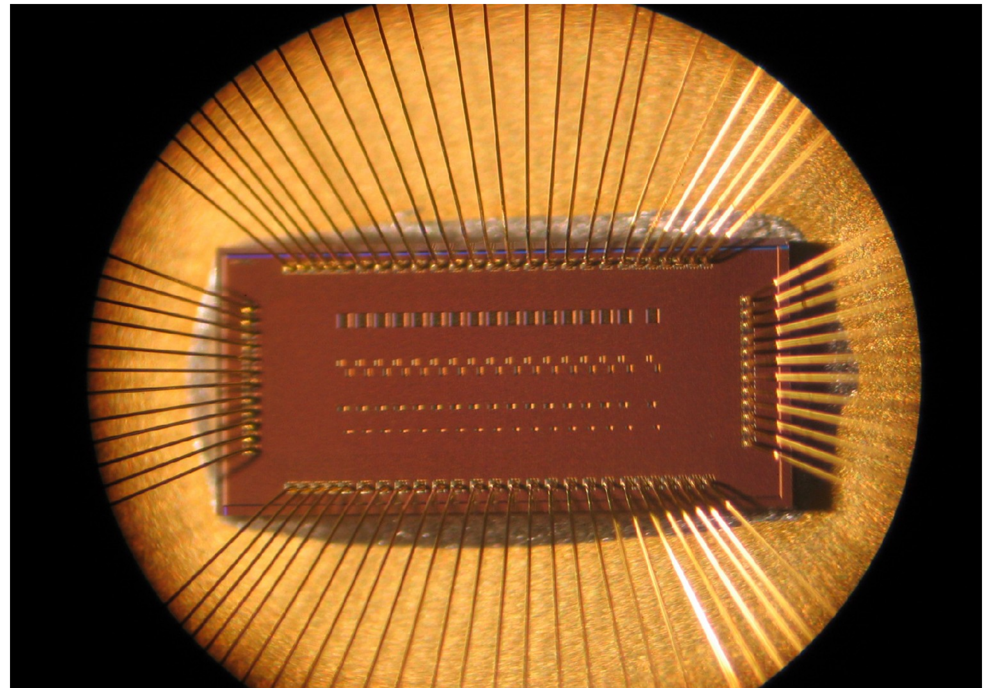


- Low noise amplification + pulse shaping
- Sample & hold
- Comparator

Submitted end '04

Silicon

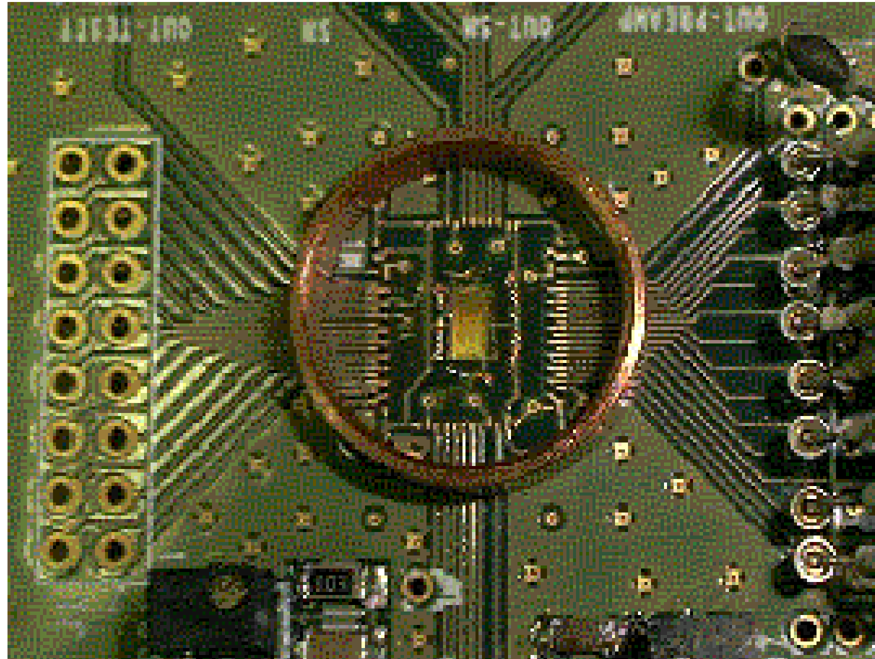




3mm

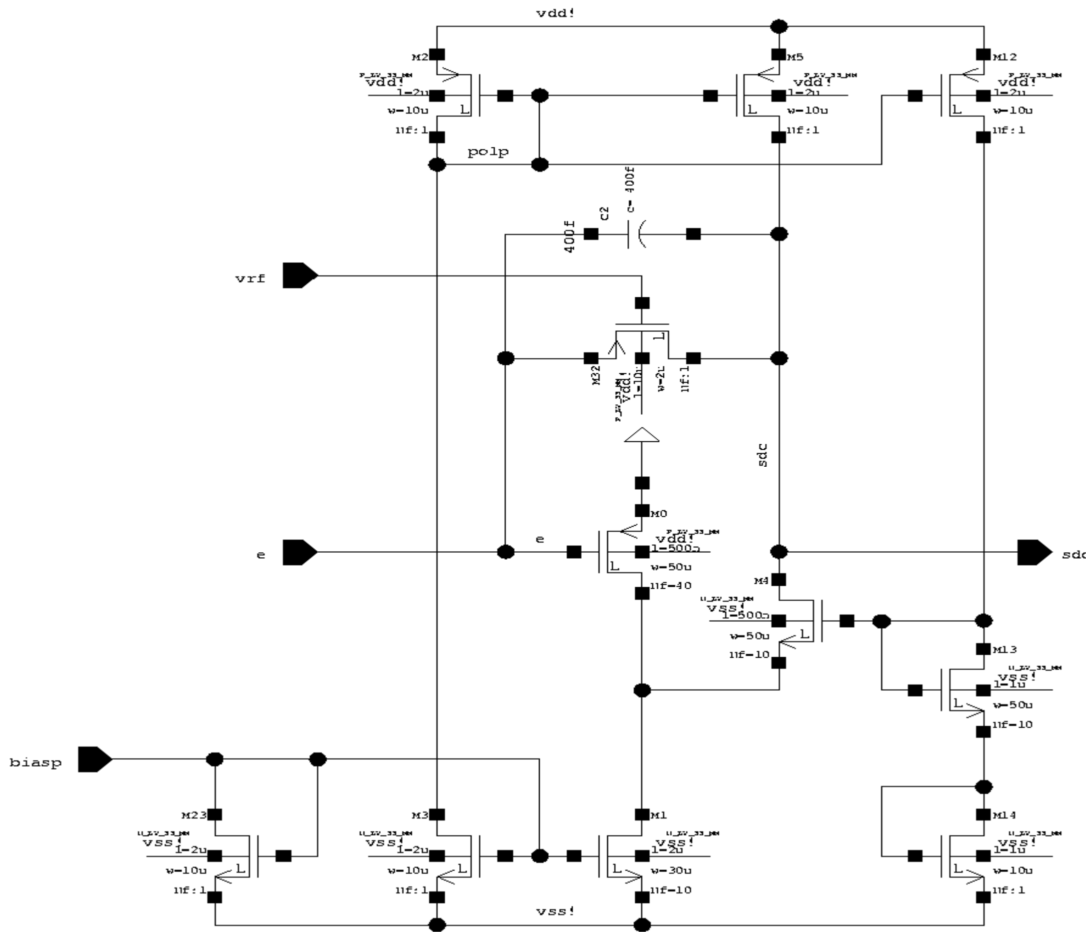
16 + 1 channel UMC 0.18 um chip (layout and picture)

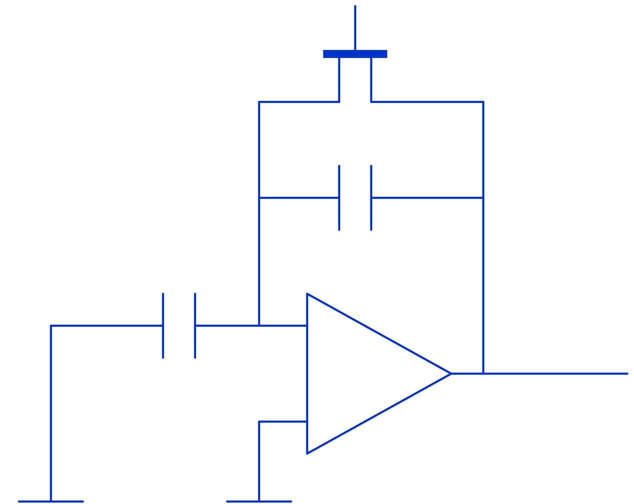
Test Card



Chip on Board version (wire bonded)

Preamp





Gain: 8mV/MIP
3.3V input transistor 2000/0.5
gm = 0.69 mA/V
40 µA current (Weak inversion
IC ~= 0.01)

Preamp tests results

Mainly OK

- Gain OK
- Linearity over :

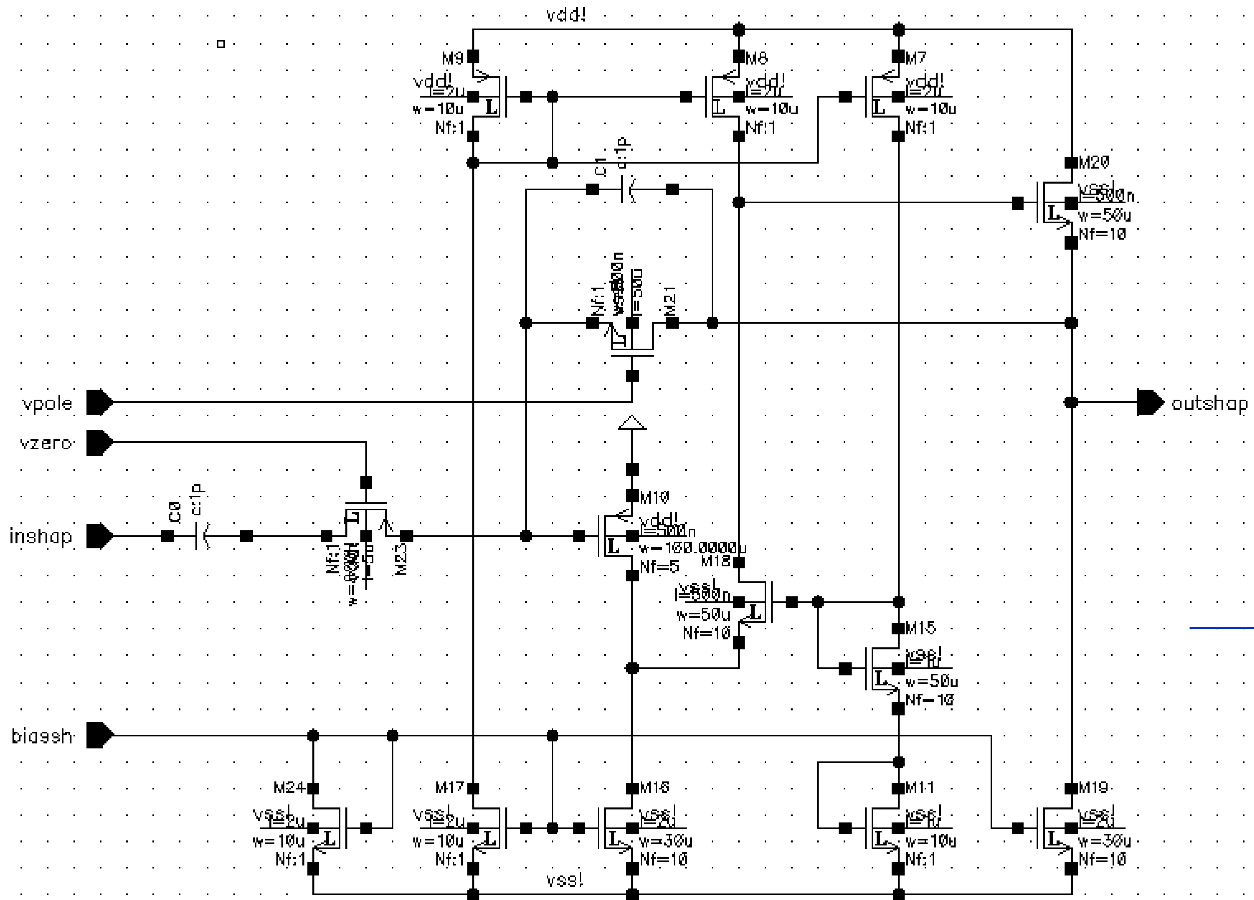
  +/-1.5% +/-0.5% expected

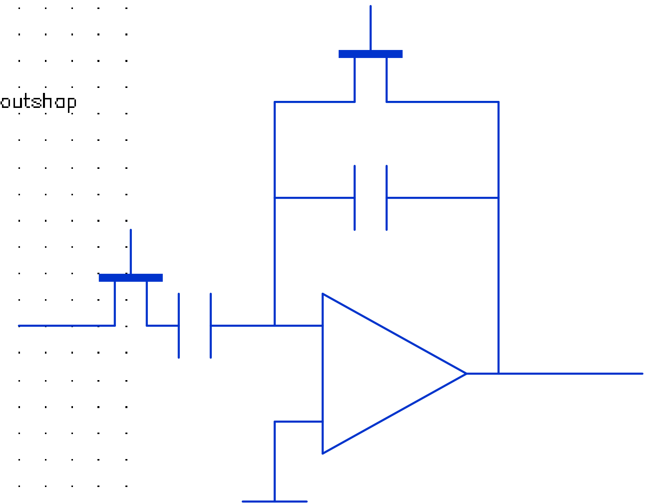
- Noise 3μs-20μs rise-fall times, 40 μA biasing:

  498 + 16.5 e-/pF OK

- Dynamic range 60 OK

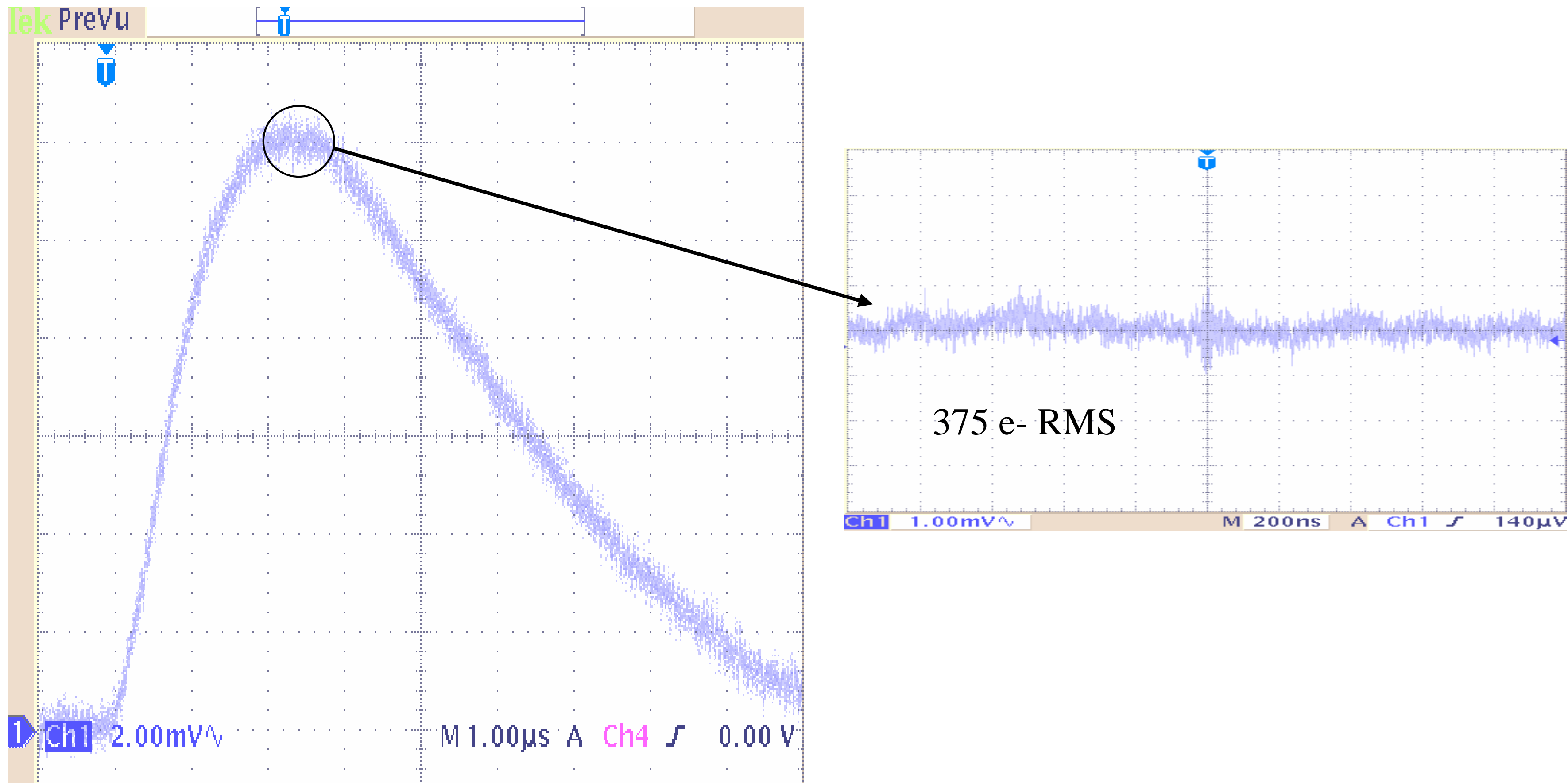
Shaper





CR-RC 1-5µs

Shaper Noise



375 e- input noise with chip-on-board wiring (against 280 simulated)

Shaper tests results

- Peaking time:

  1.5 - 6 μs tunable peaking time 1-10 targeted

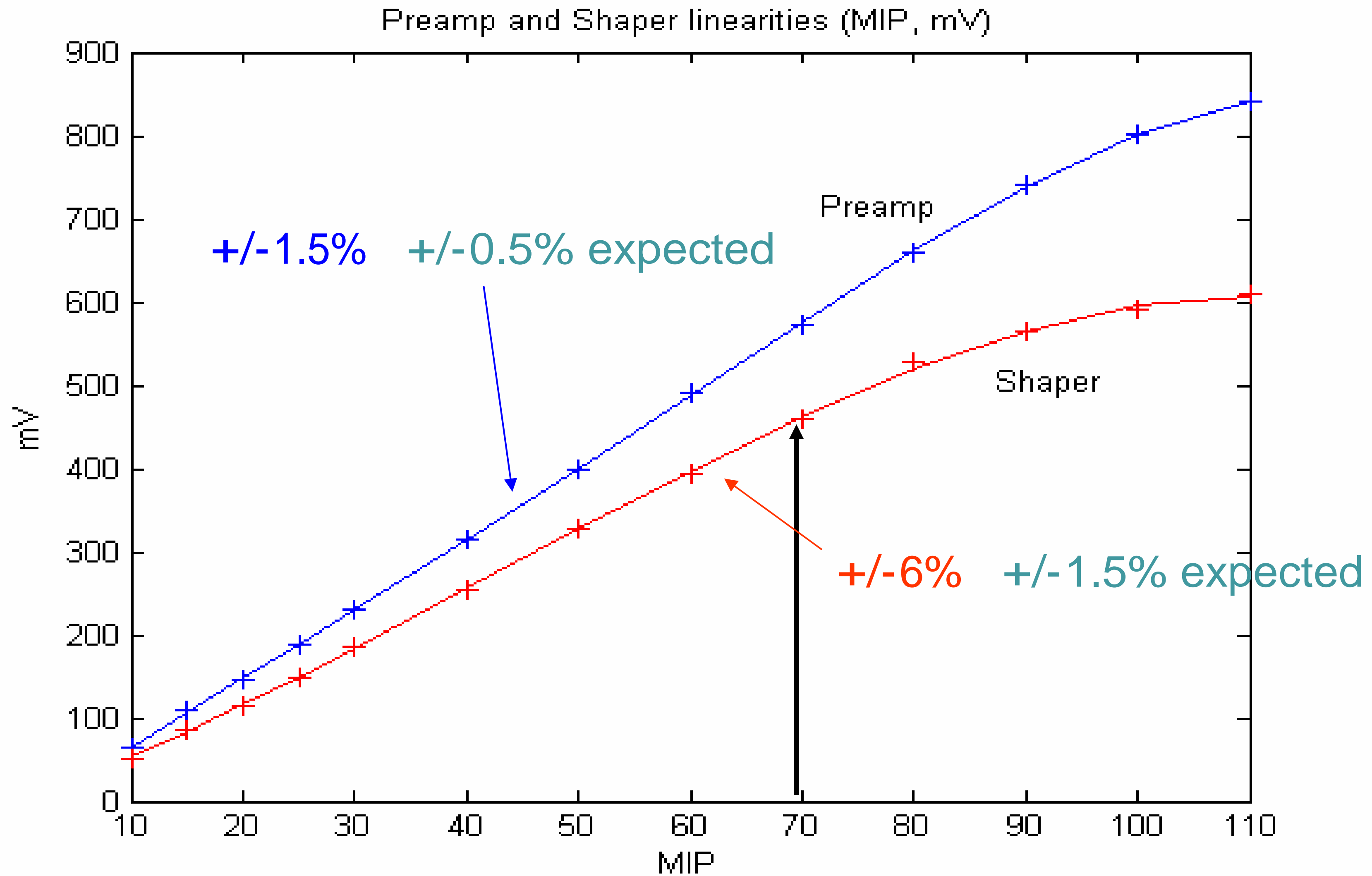
  Linearity: +/- 6% +/- 1% targeted

- Noise @ 3 us shaping time and 140μW power:

  375 + 10.4 e-/pF 274 + 8.9 e-/pF expected

- Linearity:
  +/-1.5% +/-0.5% expected

Linearities



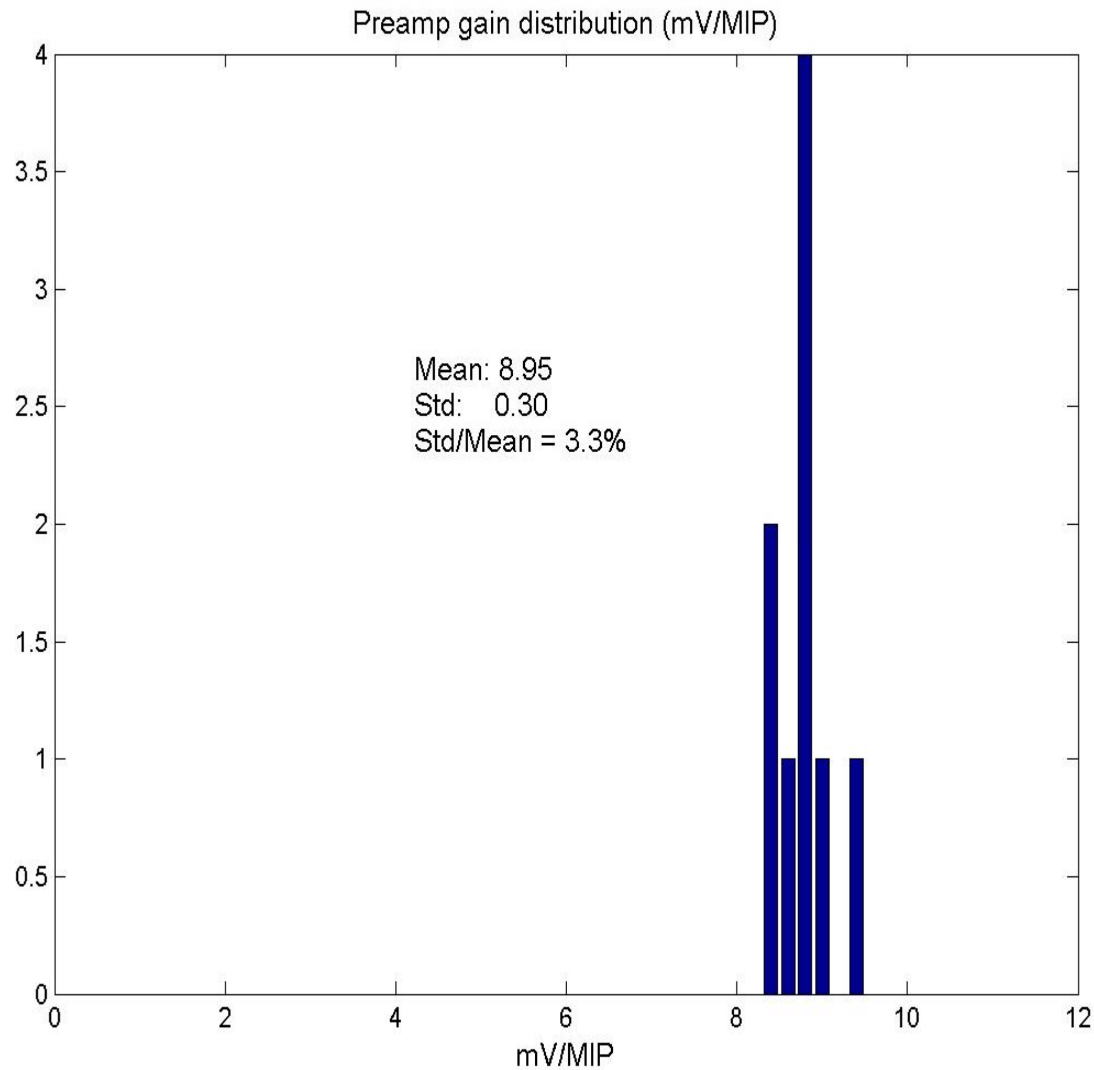
Sample & Hold Comparator

- Sample and hold: OK
- Comparator:

Vt spreads of the order of 5 mV due to transistors size

- Increase from 10/0.5 to 200/10 to reduce spreads
- Increase Preamp + Shaper voltage gain from 8 to 20 mV/MIP

Process spreads



Preamp gains statistics

Process spreads: 3.3 %

Tests Conclusions

12 chips tested (June '05)

The UMC CMOS 180nm process is mature and reliable:

- Models mainly OK
- Only one transistor failure over 12 chips
- Process spreads of a few %

Encouraging results regarding CMOS DSM

→ go to 130nm

CMOS 130nm chip design

Front-end in CMOS 130nm

130nm CMOS:

- Smaller
- Faster
- More radiation tolerant
- Lower power
- Will be (is) dominant in industry

Drawbacks:

- Reduced voltage swing (Electric field constant)
- Leaks (gate/subthreshold channel)
- Models more complex, not always up to date
- Crosstalk (digital)

Technology parameters

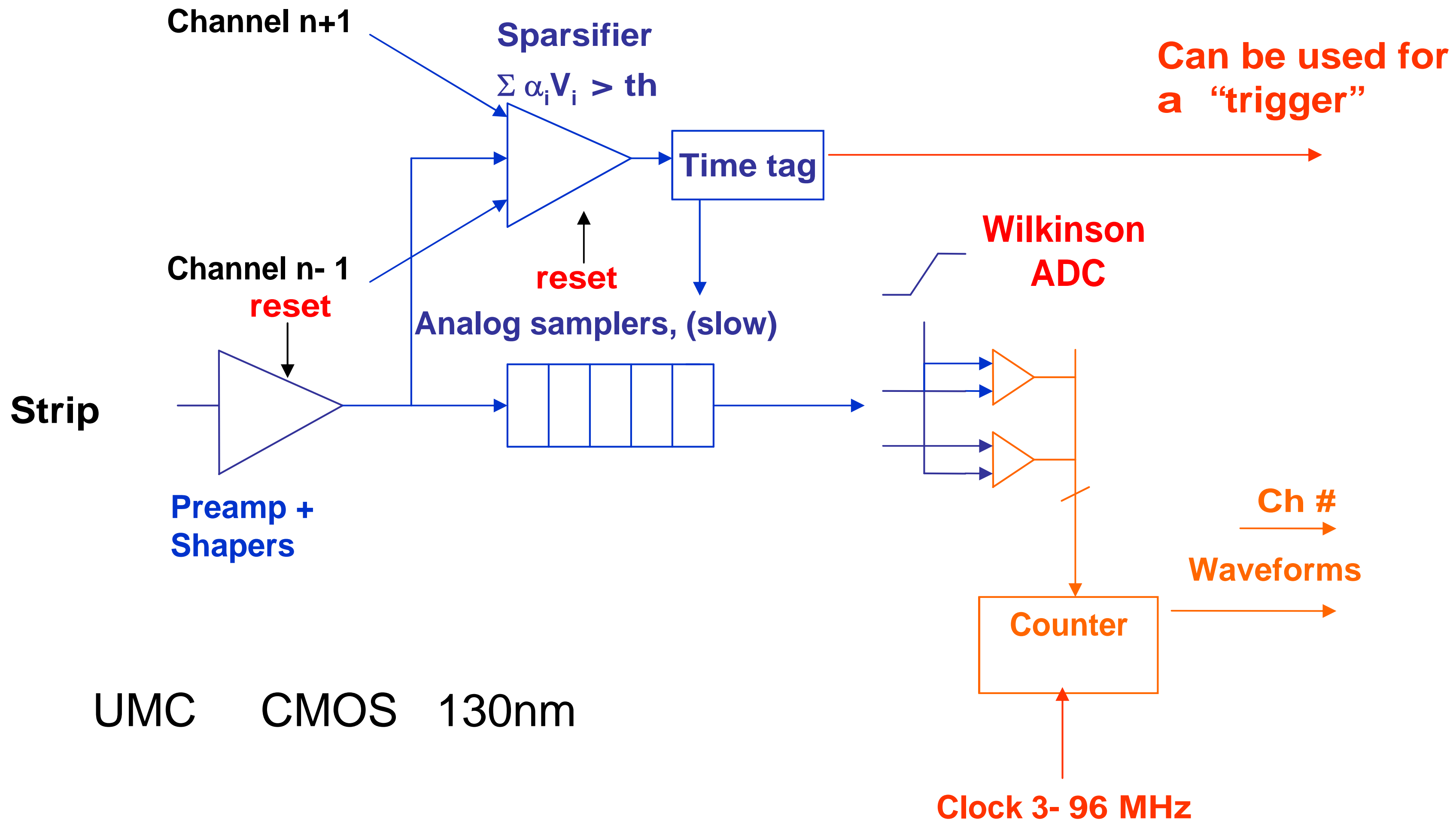
180 nm

- 3.3V transistors
- 1.8V logic supply
- 6 metals layers (Al)
- MIM capacitors = 1fF/µm²
- Three Vt options

130nm

- 3.3V transistors
- 1.2V logic supply
- 8 metals layers (Copper)
- MIM capacitors =1.5fF/µm²
- Same Vt options
- Low leakage transistors option

4-channel test chip

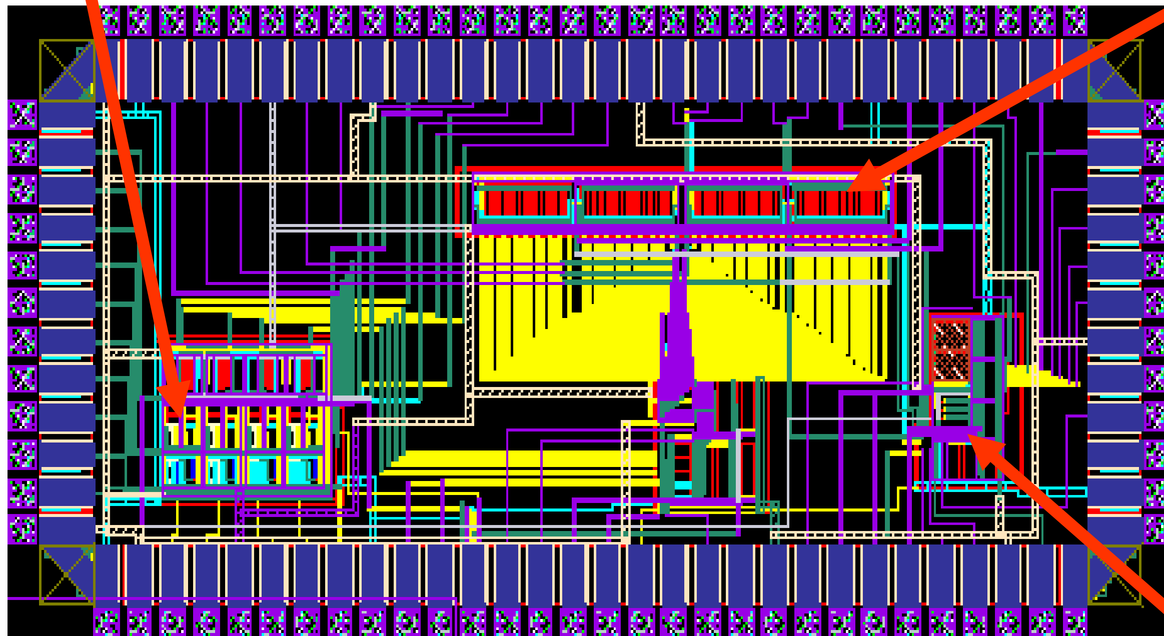


UMC CMOS 130nm

130nm CMOS chip

Amplifier, Shaper, Sparsifier 90*350 µm2

Analog sampler 250*100 µm



A/D 90*200 µm

Layout of the 130nm chip including sampling and A/D conversion

Submitted April 19th '06

Some issues with 130nm design

- Noise not properly modeled:
  1/f noise out of belief…(both coefficient and exponent)

- Design rules more constraining
- Lower power supplies voltages
  Low Vt transistors leaky

- Some (via densities) not available under Cadence (Mentor)

Front-End Digital

- Chip control
- Buffer memory
- Processing for
  - Calibrations
  - Amplitude and time least squares estimation, centroids
  - Raw data after zero suppression lossless compression
- Tools
  - Digital libraries in 130nm CMOS available
  - Synthesis from VHDL/ Verilog
  - SRAM memory
  - PLLs

Future plans

Future plans

- Implement the fast (20-100ns shaping) version with Silicon-Germanium / CMOS including:

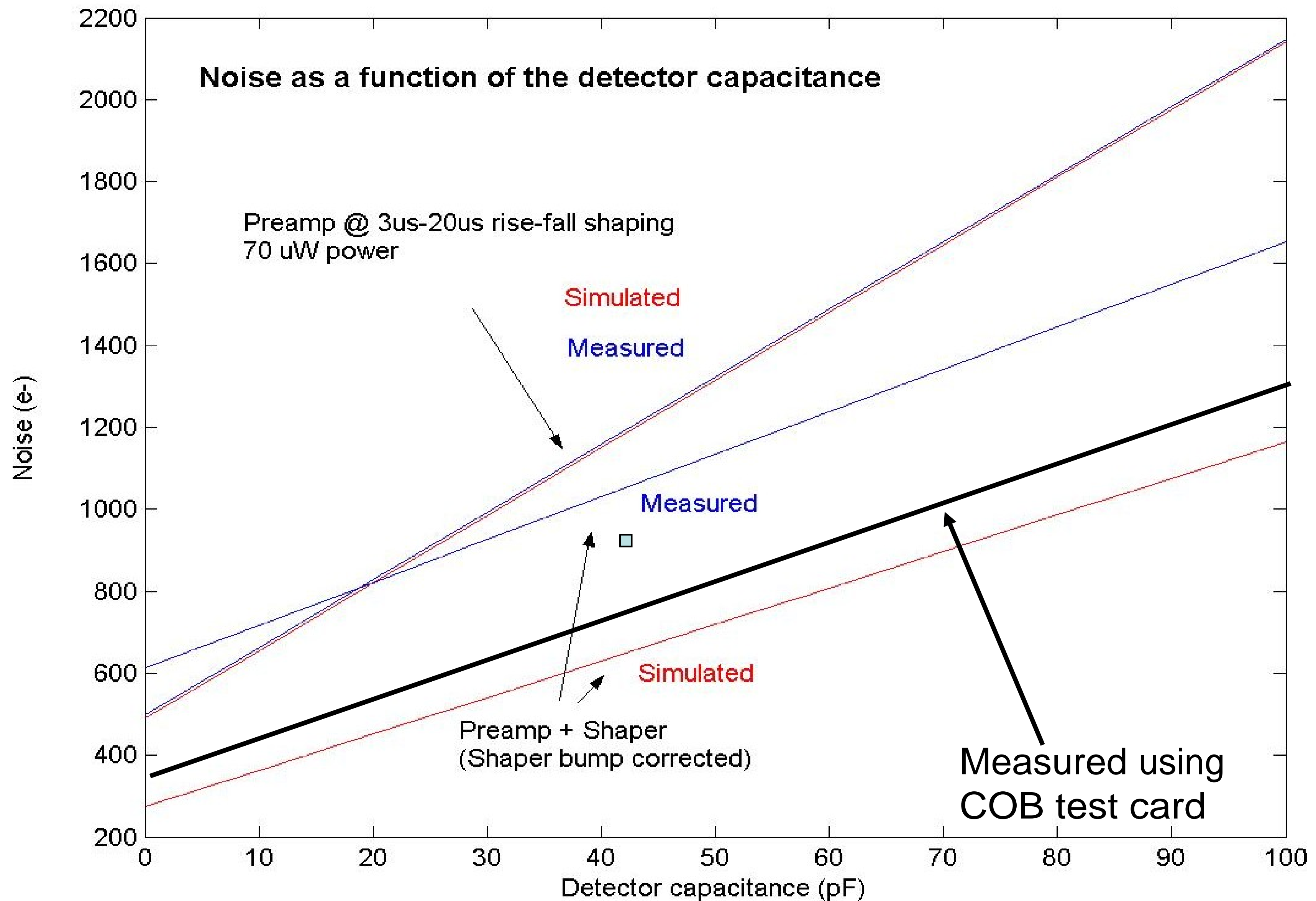
  - Preamp + Shaper (20-100ns)
  - Fast sampling
  - Power cycling

- Submit a full 128 channel version including slow and fast analog processing, power cycling, digital

The End …

Backup

Noise summary



Possible issues: Transistors leaks

Two situations:

- **Gate- channel due to tunnel effect (can affect noise performances)**
- **Through channel when transistor switched- off (only affects large digital designs)**

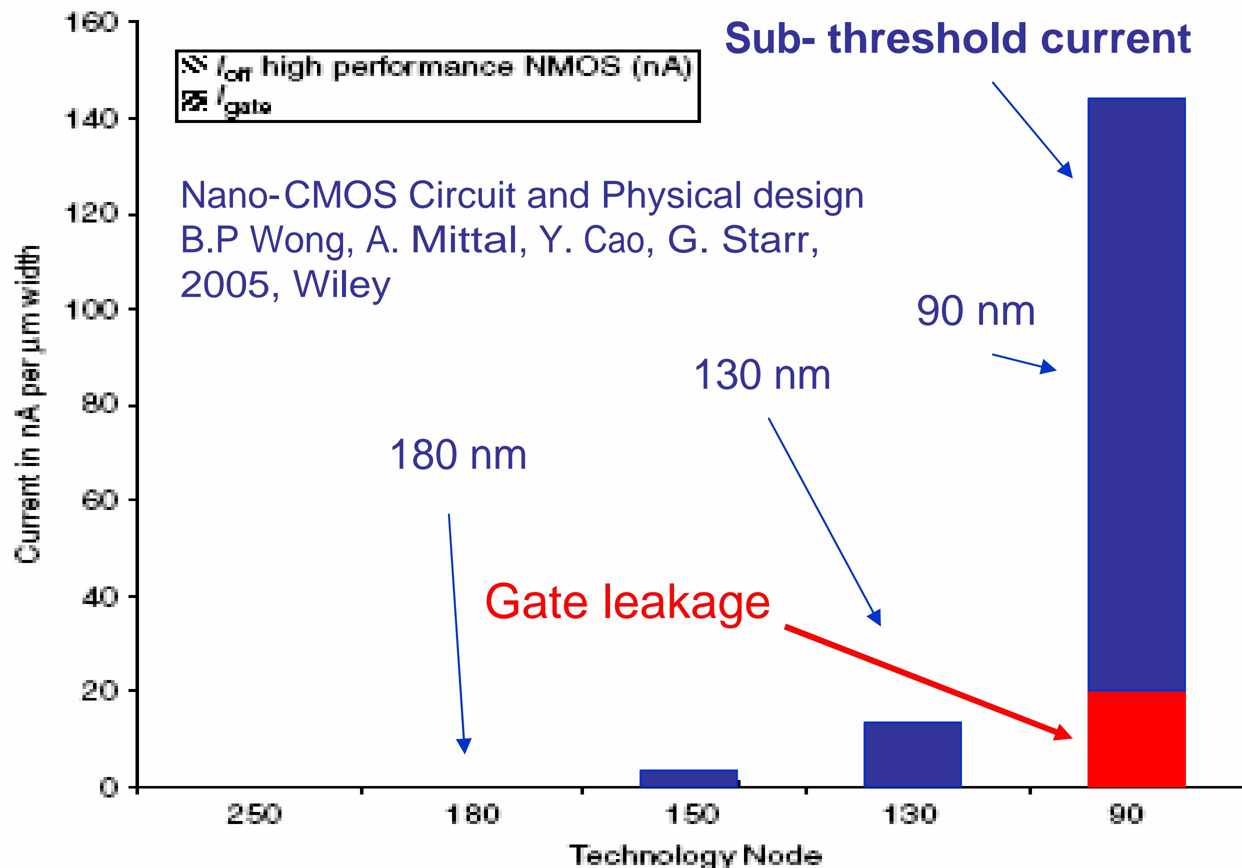


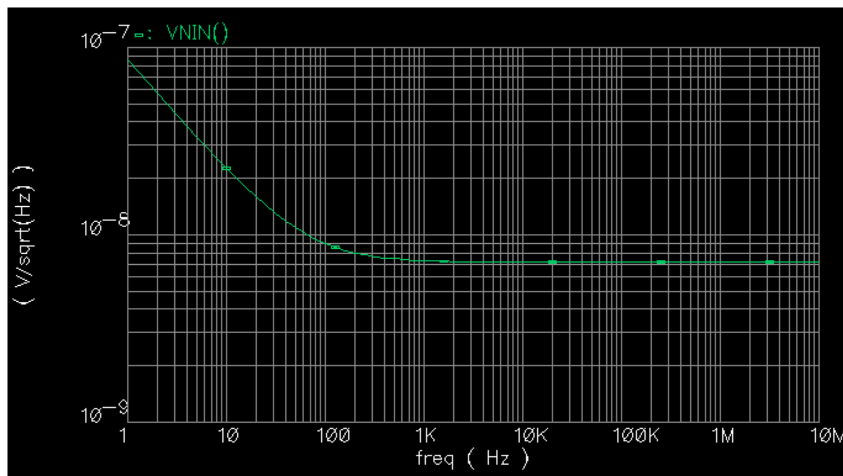
Figure 1.2 I_{gate} and subthreshold leakage versus technology.

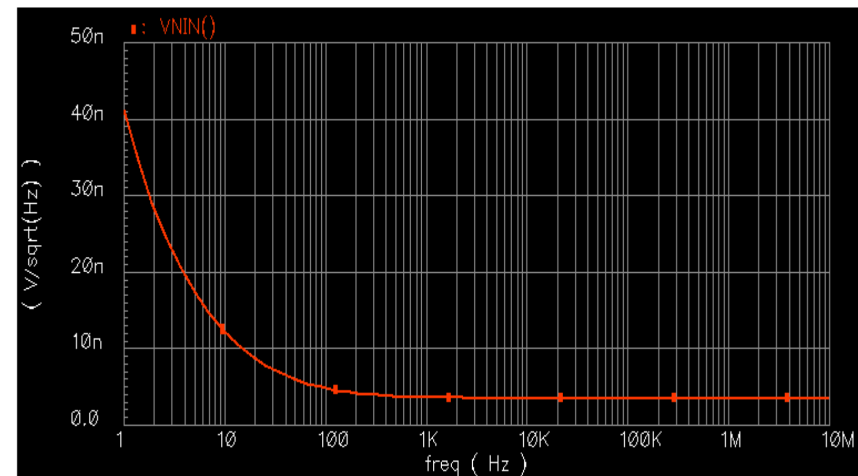
- 180nm chip OK
- 130nm, no gate leakage expected, but sub-threshold
- 90nm, important gate leakage

Scale:
1 nA/ µm = 8000 e- noise in FE

Possible issues: noise: 130nm vs 180nm (simulation)

- **PMOS:**





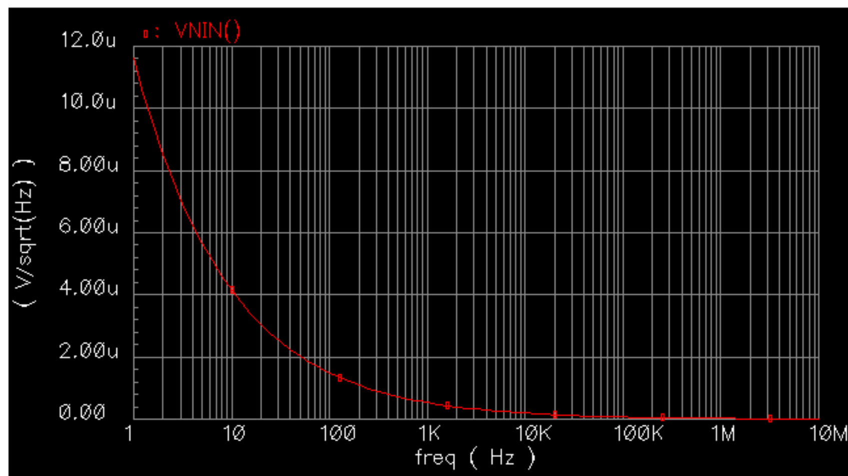
130nm
W/L = 2mm/0.5u
Ids = 38.79u,Vgs=-190mV,Vds=-600mV
gm=815.245u,gms=354.118u
1MHz → 7.16nV/sqrt(Hz)
Thermal noise hand calculation = 3.68nV/sqrt(Hz)

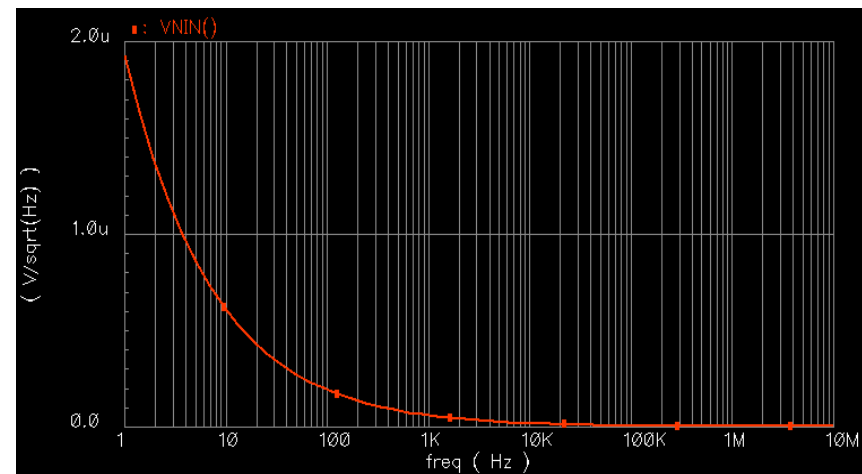
180nm

gm=944.4uS,gms=203.1uS
1MHz → 3.508nV/sqrt(Hz)
Thermal noise hand calculation = 3.42nV/sqrt(Hz)

Noise: 130nm vs 180nm (simulation)

NMOS :





130nm
W/L = 50u/0.5u
Ids=48.0505u,Vgs=260mV,Vds=1.2V
gm=772.031uS,gms=245.341uS,gds=6.3575uS
1MHz --> 24.65nV/sqrt(Hz)
100MHz --> 5nV/sqrt(Hz)
Thermal noise hand calculation = 3.78nV/sqrt(Hz)

180nm
W/L=50u/0.5u
Ids=47uA,Vgs=300mV,Vds=1.2V
gm=842.8uS,gms=141.2uS,gds=16.05uS
1MHz --> 4nV/sqrt(Hz)
10MHz --> 3.49nV/sqrt(Hz)
Thermal noise hand calculation = 3.62nV/sqrt(Hz)

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