Timepix, a pixel readout chip for arrival time measurements in a TPC*

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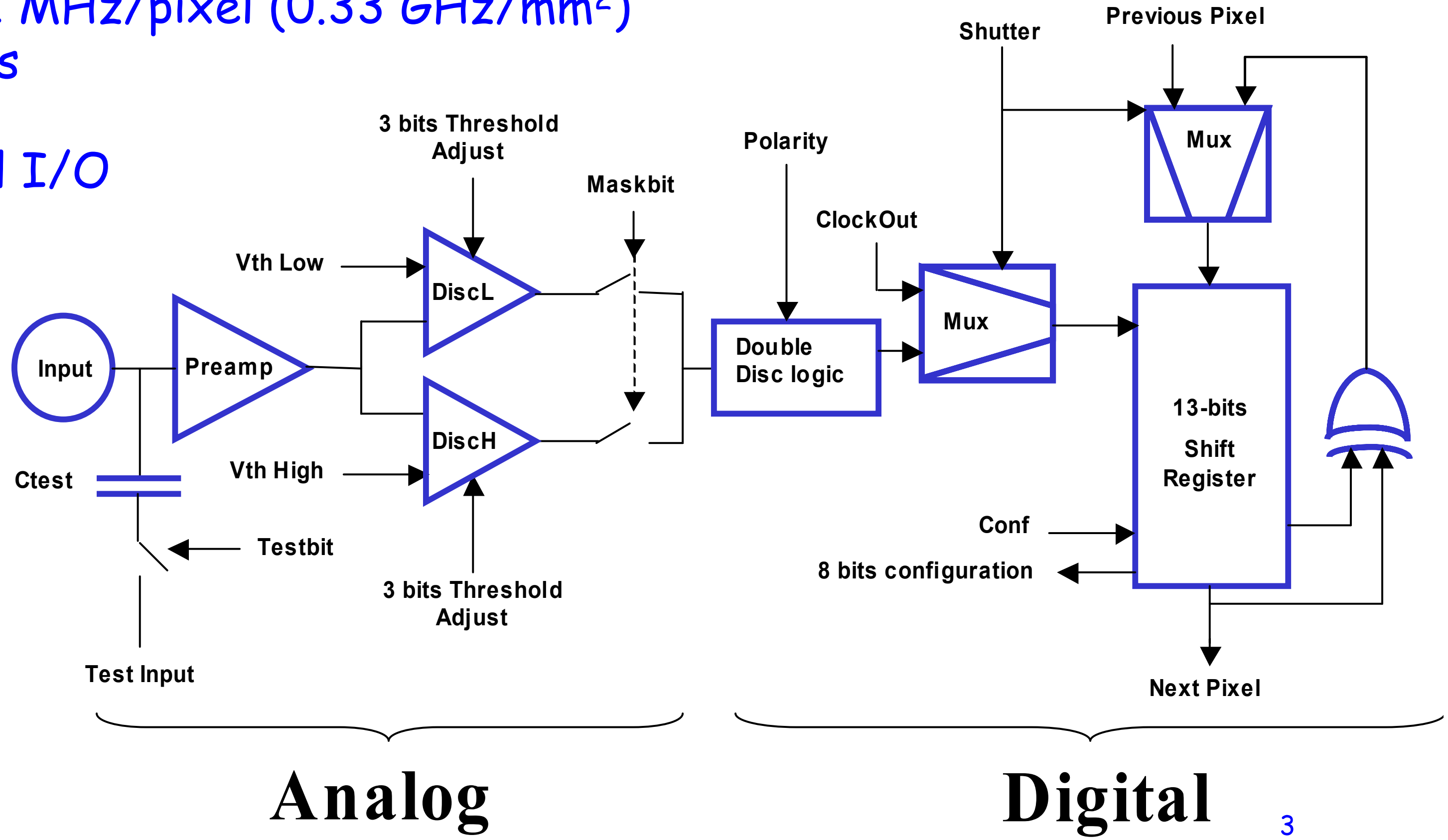
* This work is carried out in the framework of the Medipix2 Collaboration
with the financial support and guidance of the EUDet Collaboration

Outline

- Medipix2: Brief description and some results
- From Medipix to Timepix
- How to generate a 10ns time stamp?
- Timepix schematic proposal and simulations
- Summary

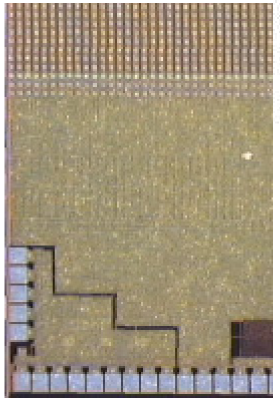
A bit of history…2001

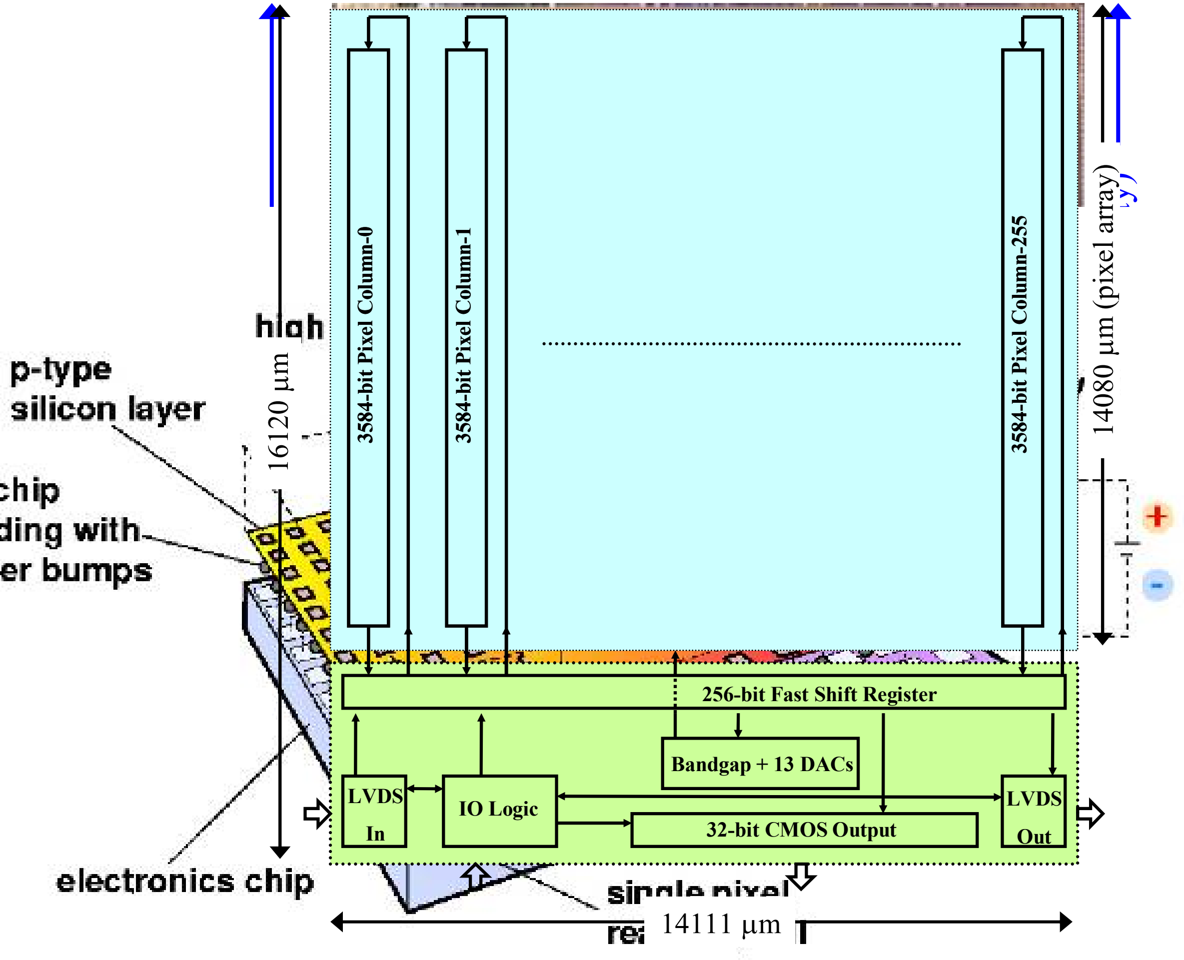
- Square pixel size of 55 μm
- Sensitive to positive or negative input charge
- Pixel by pixel detector leakage current compensation
- Window in energy as precise as possible
- 14-bit counter per pixel with overflow control
- Count rates of 1 MHz/pixel (0.33 GHz/mm^2)
- 256 x 256 pixels
- 3-side buttable
- serial or parallel I/O



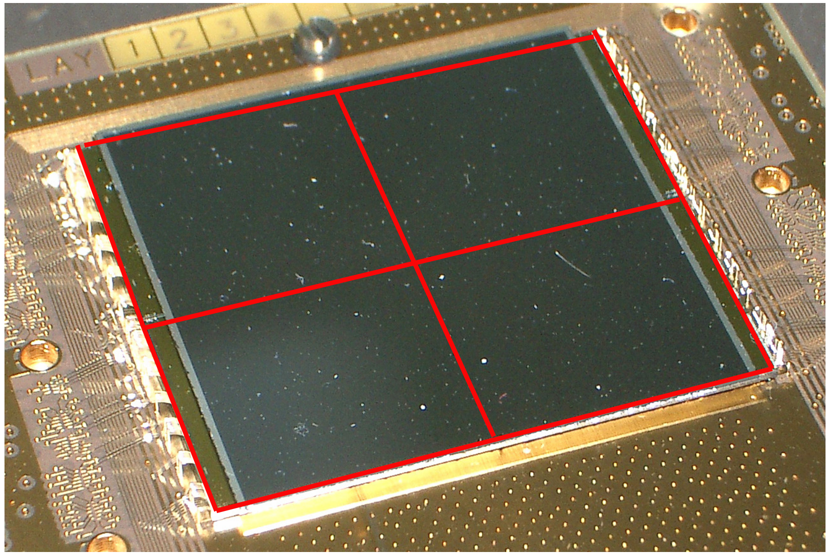
A bit of history…

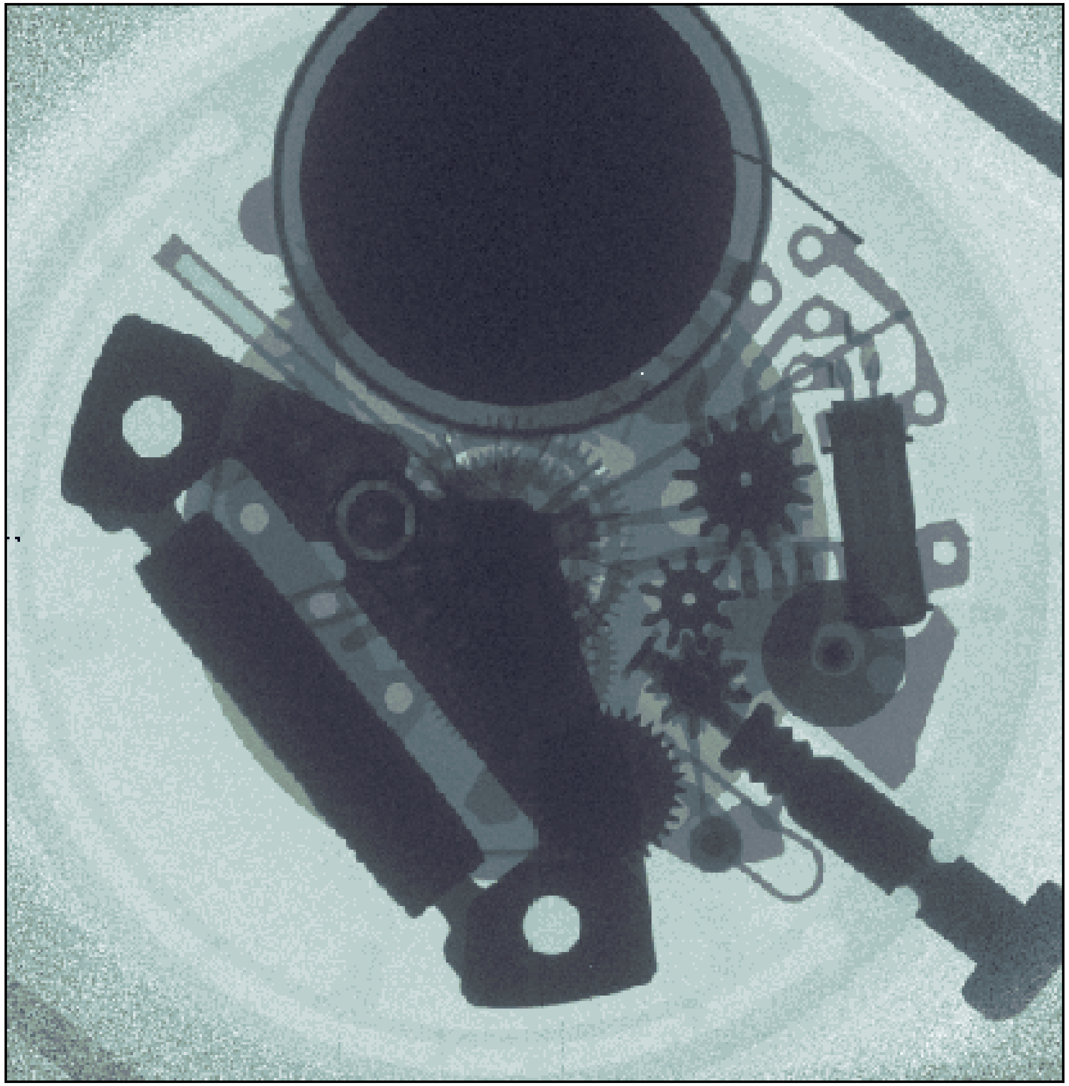
- 6 metal layers IBM 0.25um
- Serial readout <5ms@180MHz
- Parallel readout <300us@120MHz (>1KHz frame !!!)
- Static power consumption ~250mA
- >35 Mtrts
- http://www.cern.ch/Medipix





Some results…

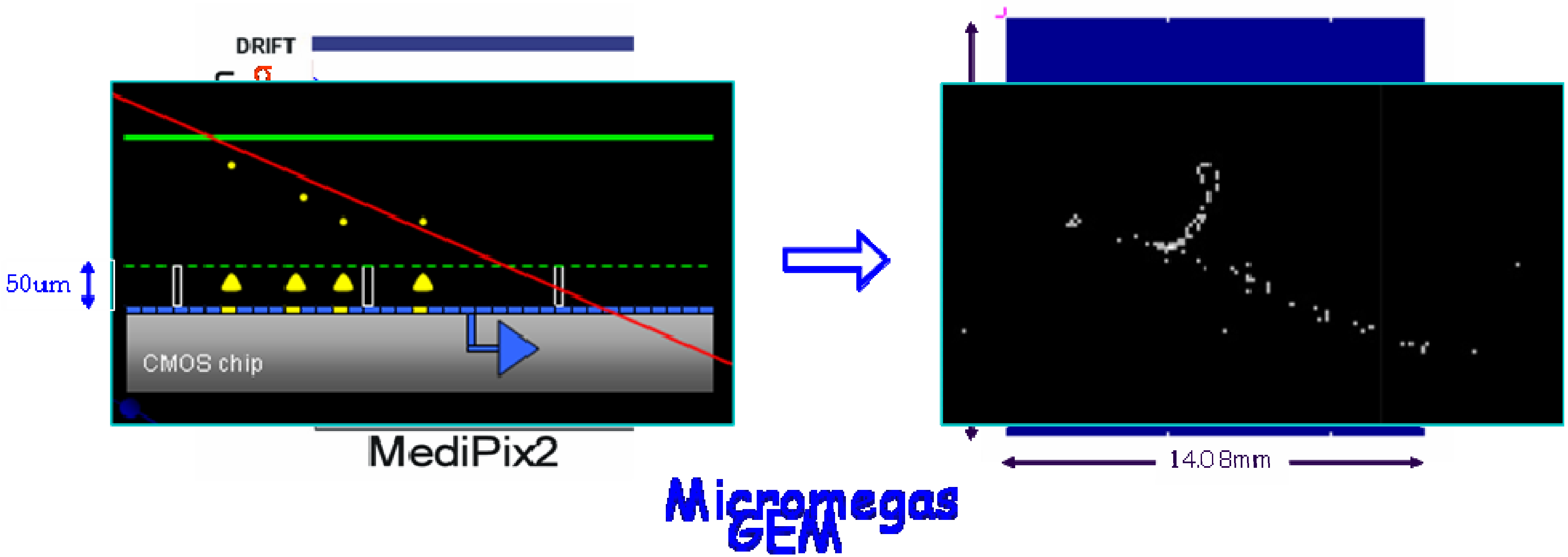




- Medipix2 Quad ⇒ 264kpixels !!
- Minimun Threshold ⇒ ~4KeV
- A ticking wrist watch have been taken with a Medipix2 Quad with 5.5fps (100ms acquisition time + 80ms readout time) using a W X-ray tube@50KV.

From Medipix to Timepix

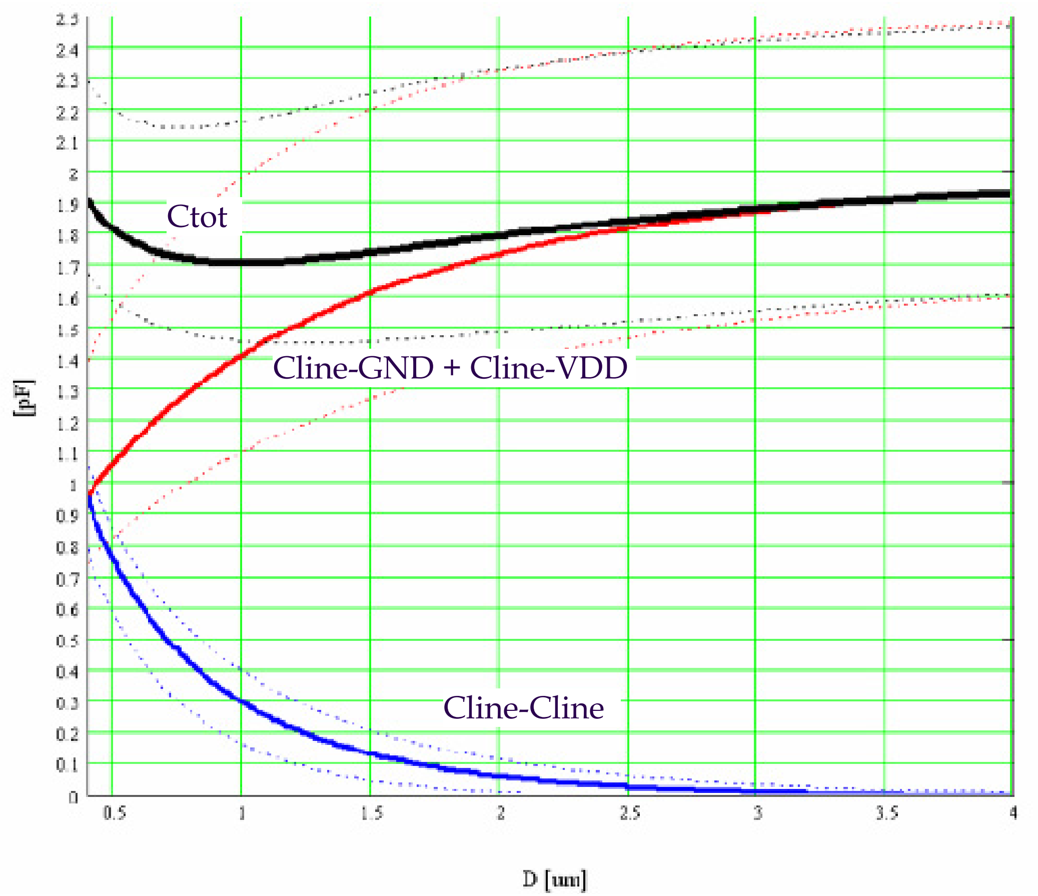
- A novel approach for the readout of a TPC at the future linear collider is to use a CMOS pixel detector combined with some kind of gas gain grid
- Using a *naked* photon counting chip Medipix2 coupled to GEMs or Micromegas demonstrated the feasibility of such approach

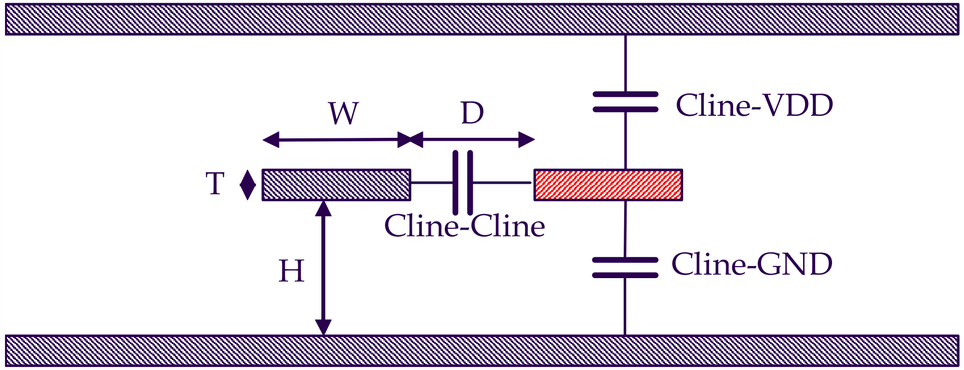


Motivation

- These experiments (by NIKHEF/Saclay, Freiburg 2004/2005) demonstrated that single electrons could be detected using a *naked* Medipix2 chip ⇒ 2D
- Did not provide information on the arrival time of the electron in the sensitive gas volume ⇒ 3D (position + time) !!!
- To further exploit this approach the Medipix2 is being redesigned to incorporate a time stamp with a tunable resolution of 100 to 10ns.
- Requirements:
  - Keep Timepix as similar as possible to Medipix2 in order to benefit from large prior effort in R/O hardware and software
  - Avoid major changes in pixel and/or readout logic - risk of chip failure due to poor mixed mode modelling
  - Eliminate 2nd threshold
  - Add possibility of programming pixel by pixel arrival time or TOT information
- This modification is supported by the JRA2/EUDET Collaboration (www.eudet.org)

Column RC characteristics

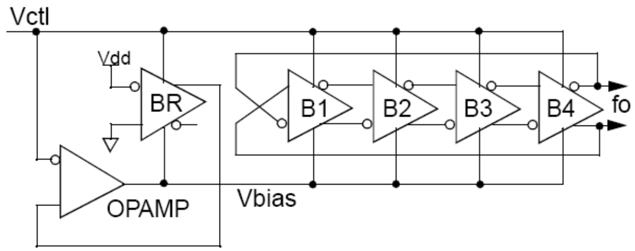




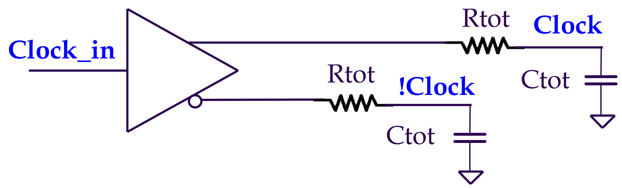
- Column length= 55x256= 14080µm
- W=0.4µm,T=0.54µm, H=0.8µm
- R≅2.8KΩ
- Ctot<=2pF
- Parasitic cap negligible at D>3 µm

Time stamp generation/distribution

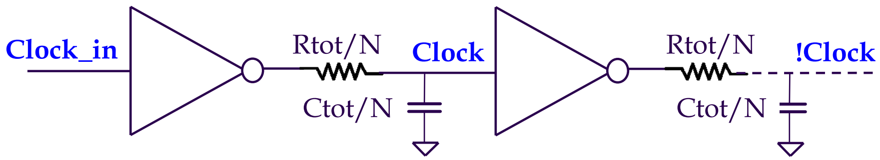
- Time stamp generated per pixel ⇒ very low power dissipation
  - Frequency controlled by voltage (DAC on chip) ⇒ compatible with Medipix readout
  - Good temperature stability <0.1%/°C
  - Moderate area consuming
  - Need of very precise frequency calibration
  - Top-down column voltage drops



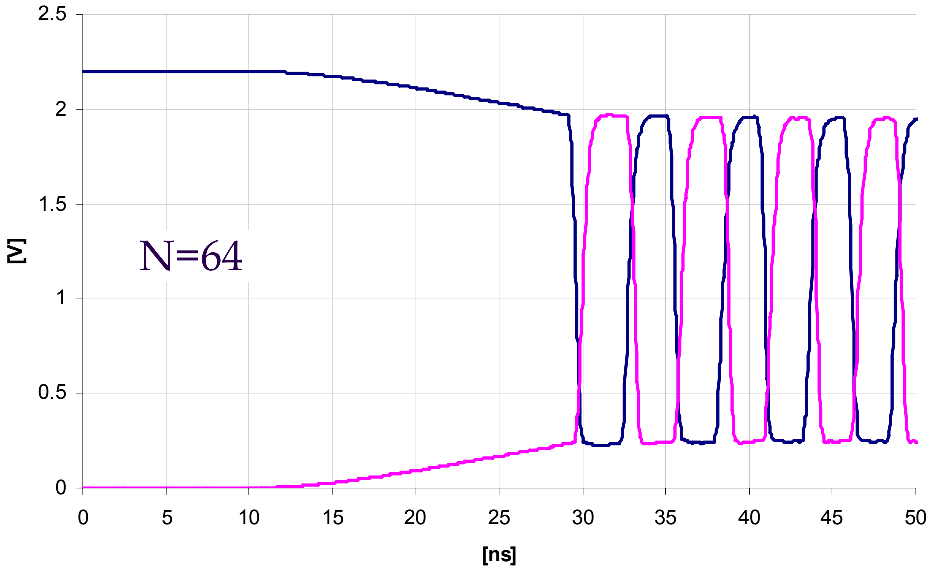
- 1 buffer per column:
  - Send a differential signal Clock and !Clock to diminish coupling
  - Bottom-Top rise/fall time effect ($R_{bot} << R_{top}$)
  - Huge Buffer to supply 100MHz
  - Non uniform power distribution over clock period

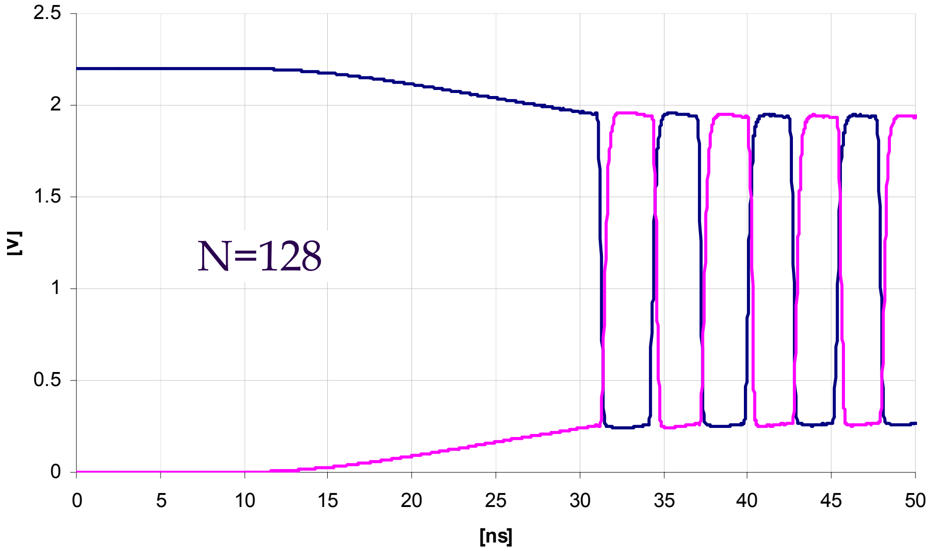


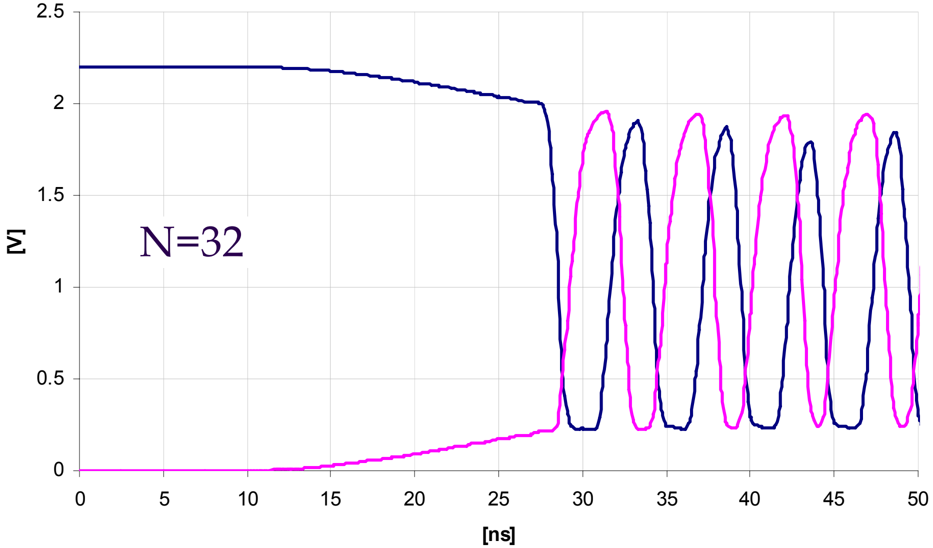
- N buffer per column:
  - Min size buffer ⇒ inverter per pixel
  - No differential signals needed
  - Power uniformly distributed over clock period



N Buffer clock distribution (2)

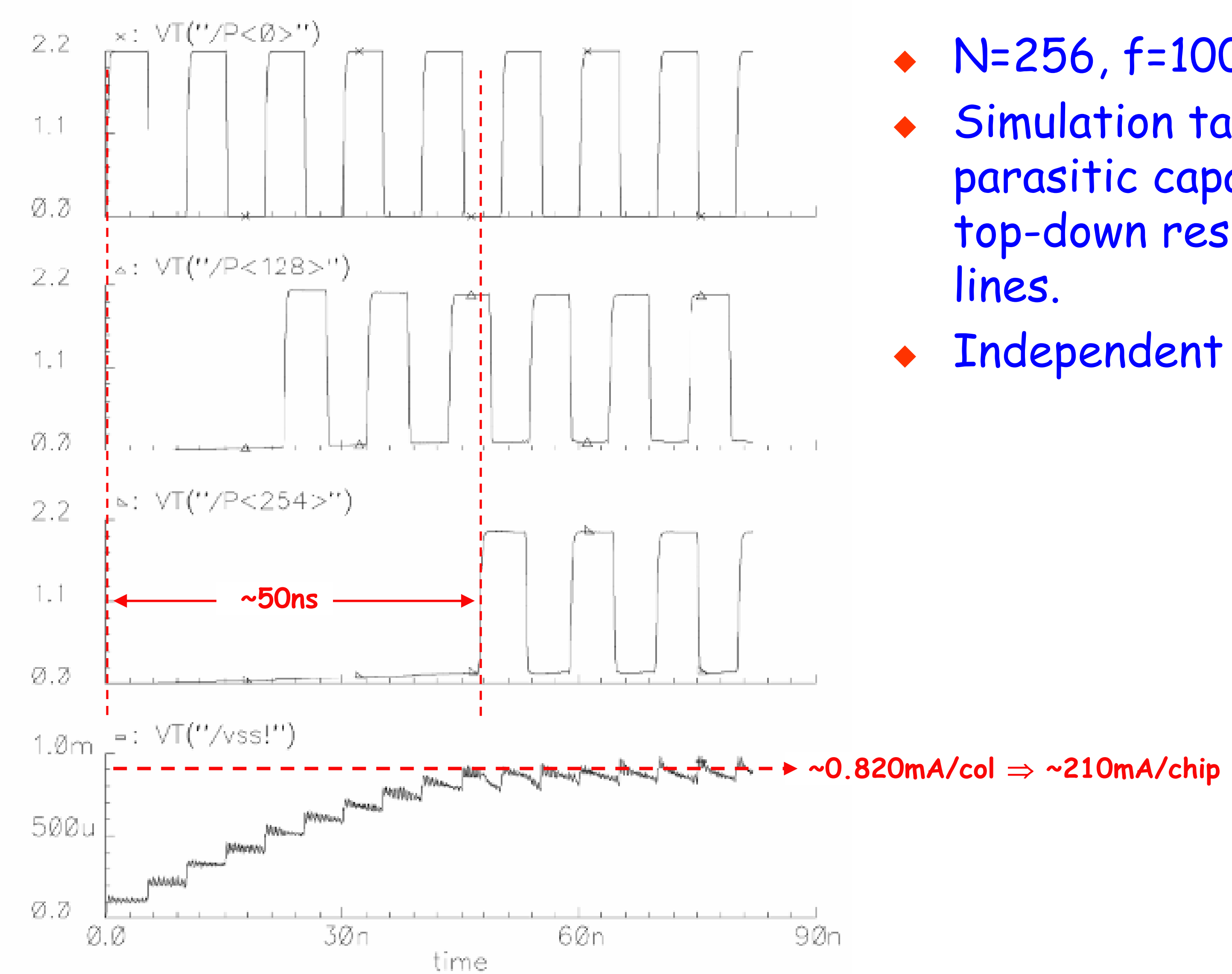






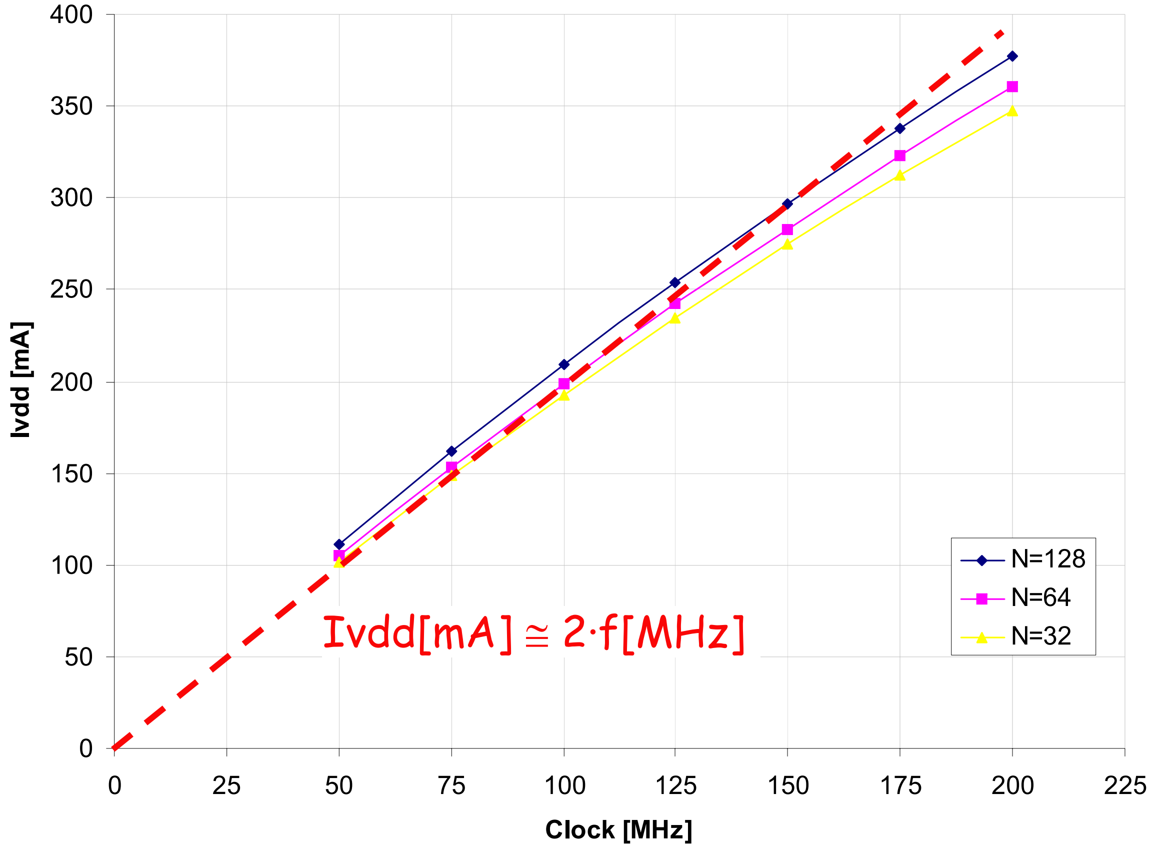
- fClock=200MHz
- Time response at the top of column

Column clock distribution propagation delay



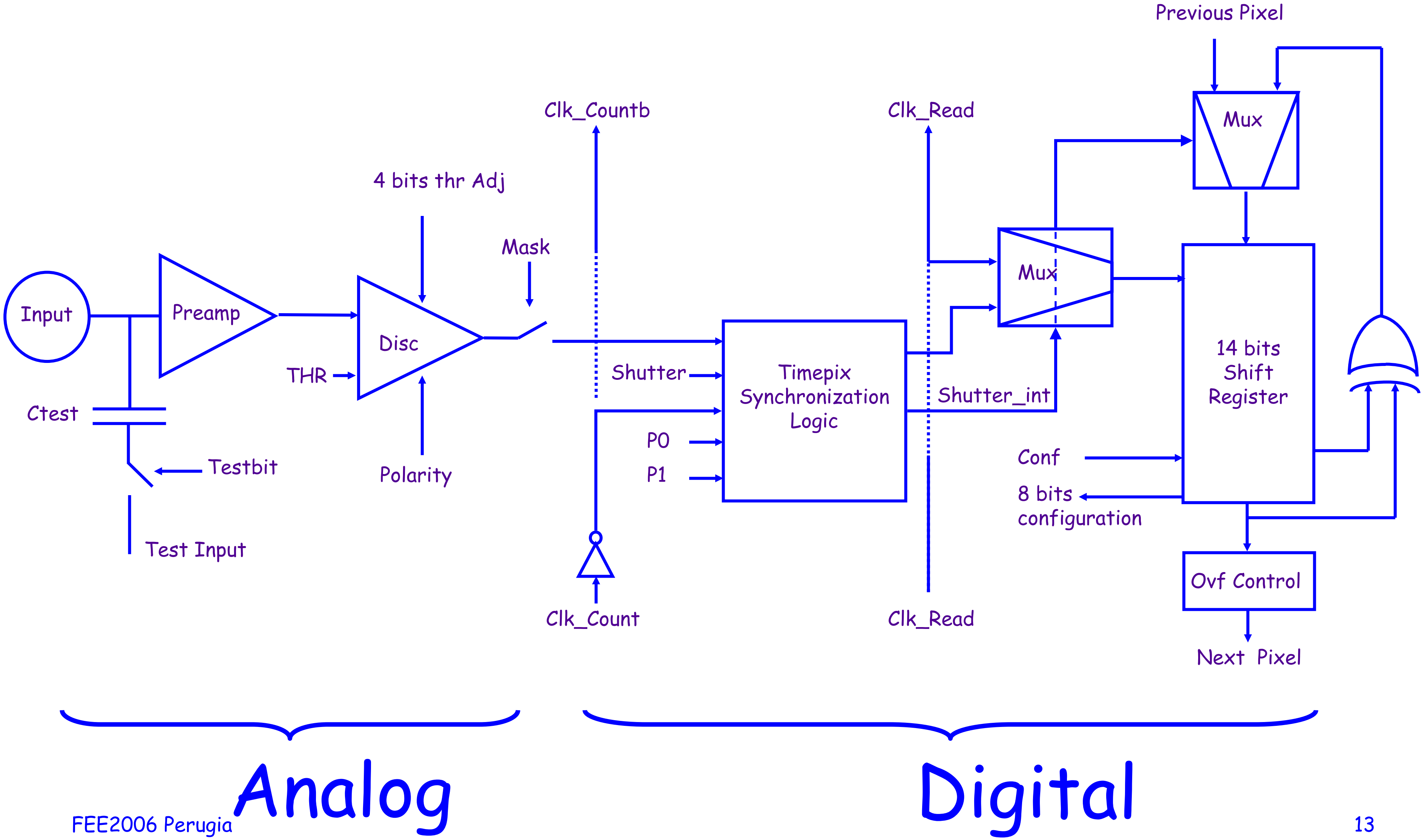
- N=256, f=100MHz
- Simulation takes care of parasitic capacitances and top-down resistive power lines.
- Independent power supply

N Buffer clock distribution



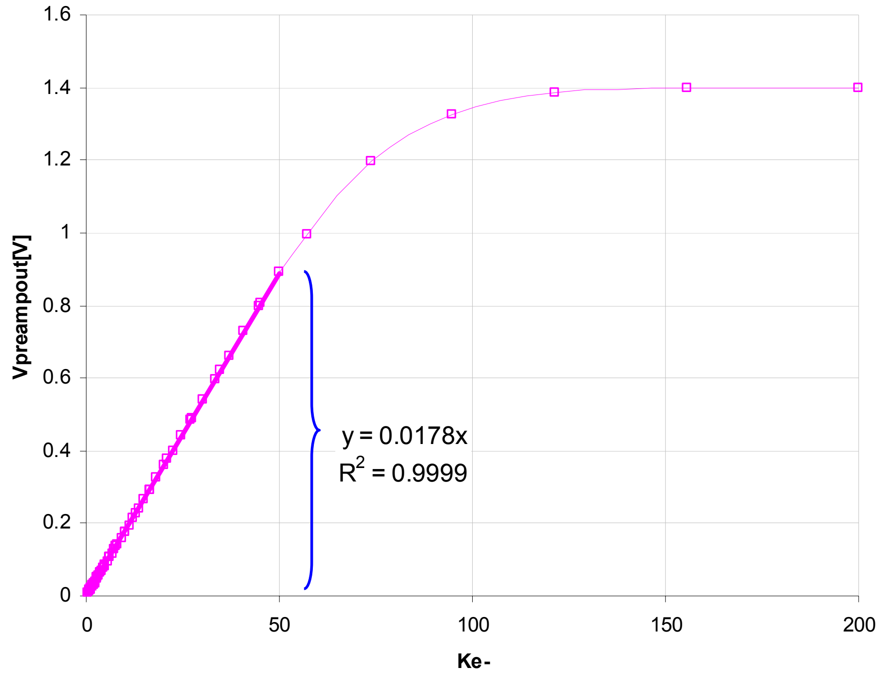
- $Ivdd=V^2 \cdot f \cdot C_{tot}$
- Simulation @ Vdd=2.2V but digital part could work to 1.8V (33% less power)

Timepix Schematic

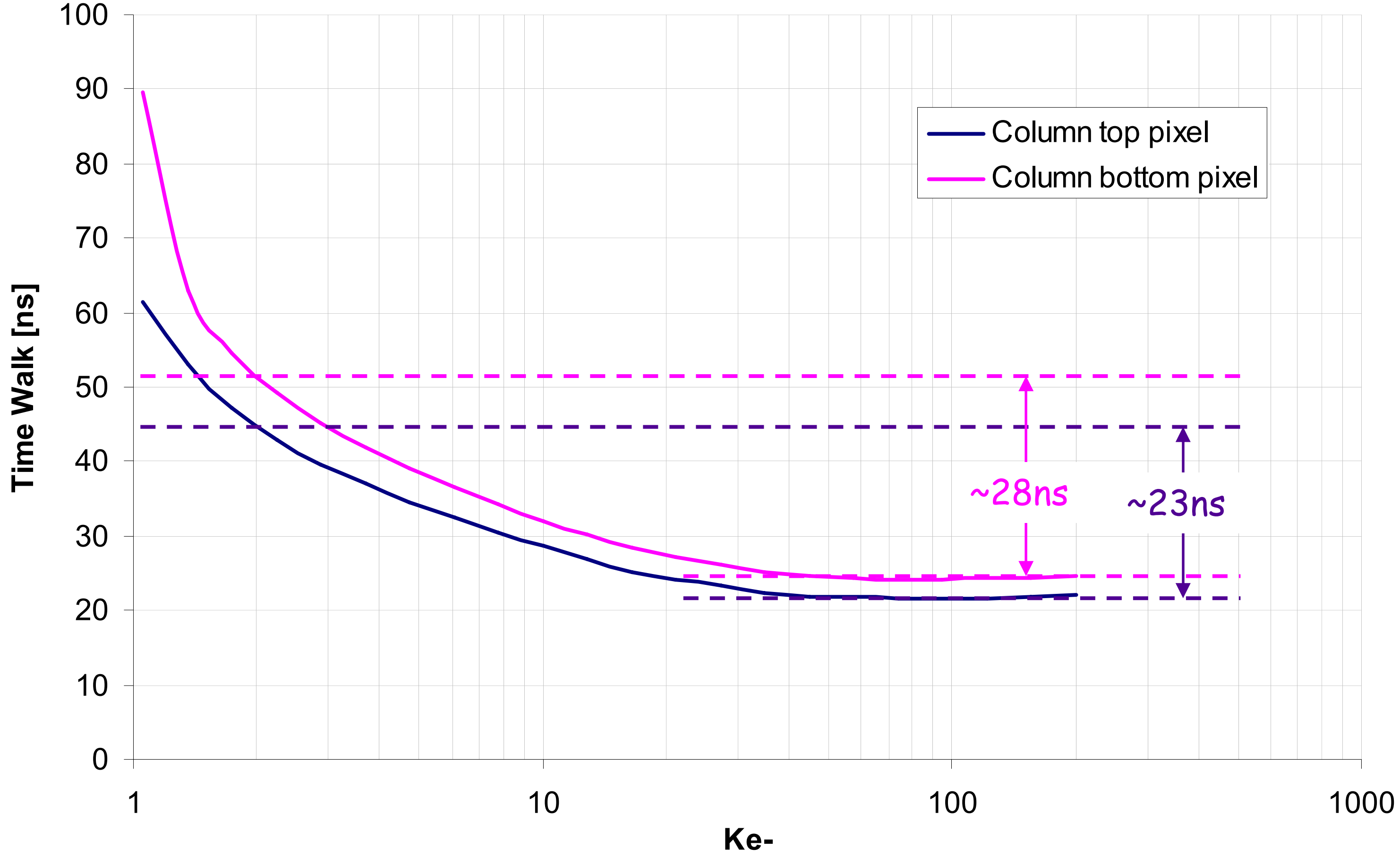


Analog Side changes

- Added cascode in preamp:
  - Gain ↑ (~18mV/Ke^-) keeping V_{outrms} noise ≅ cte ⇒ SNR ↑
  - ENC ≅ 75e^-
  - Linearity: 0.6 to 1.5 Volts ⇒ ≅50Ke^- linear range
  - Missmatch: σ_{vt} ≅ 2.11mV ⇒ σ_{vt} ≅ 117e^-

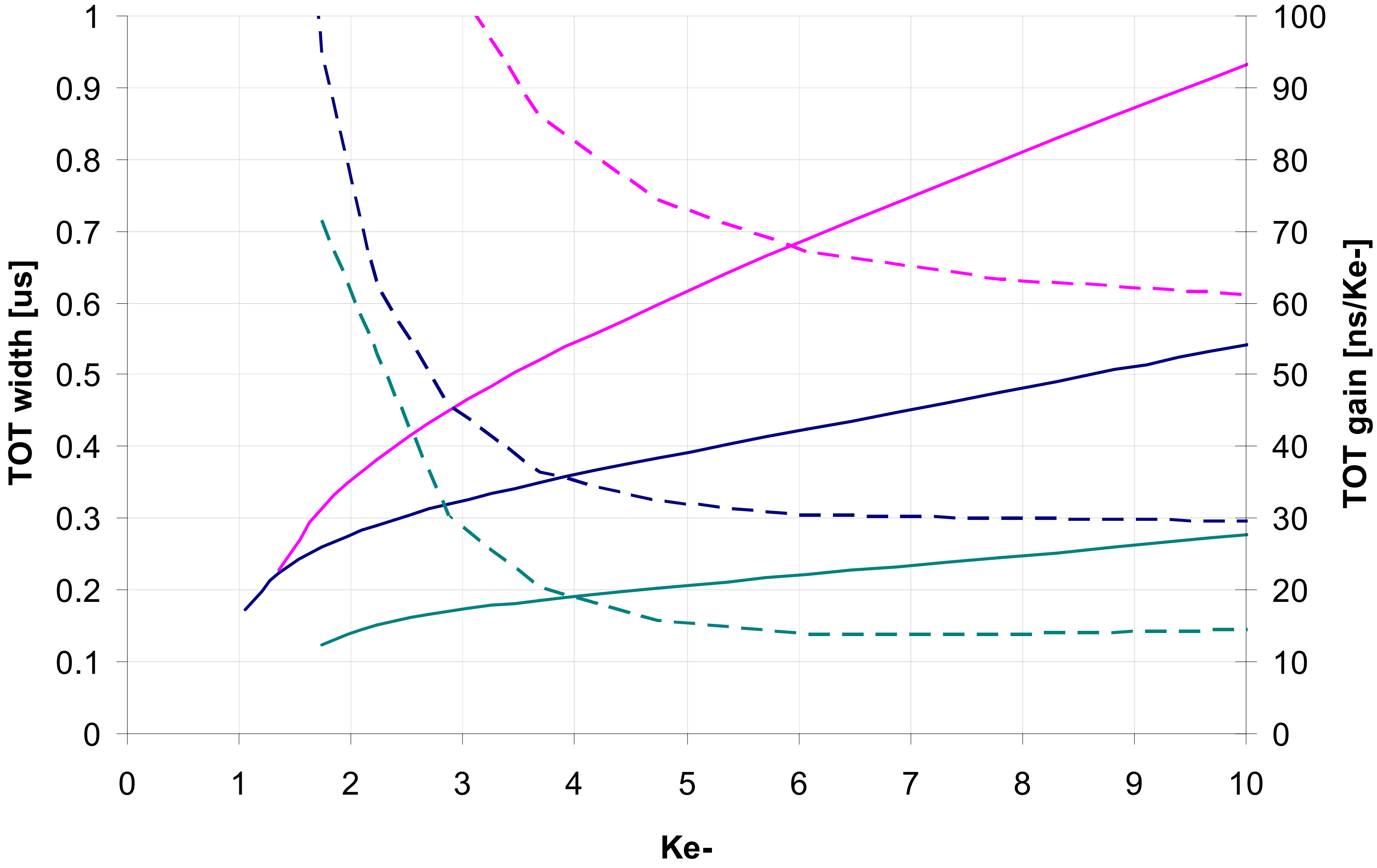


Time walk



- Threshold set at 1Ke⁻ (18mV over noise floor)
- Time walk from 2xQthr to 200Ke⁻

TOT vs Ikrum



1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
TOT width [us]
100
90
80
70
60
50
40
30
20
10
0
TOT gain [ns/Ke-]
0
1
2
3
4
5
6
7
8
9
10
Ke-

Analog pixel summary

Amplifier Gain	~18mV/Ke	
Peaking Time	90ns…140ns (IPreamp)	
Pixel noise	~75e^-_{rms}	
Preamp DC Level (FBK)	800mV (e^-)	1.4V (h^+)
Threshold dispersion	~170e^-	
Adjusted Threshold dispersion	~25e^-	
Minimum Threshold	~500e^-	
Voltage linear range	0 to 50 Ke^- (< 2%)	
TOT linear range	>200Ke^-	
Time Walk	~25ns (2Qth to ∞)	
TOTgain	~55ns/Ke^- (Ikrum=5nA)	
Analog Pixel consumption (Max)	2.9µA x 2.2V = 6.38 µW (30% less than Medipix2)	

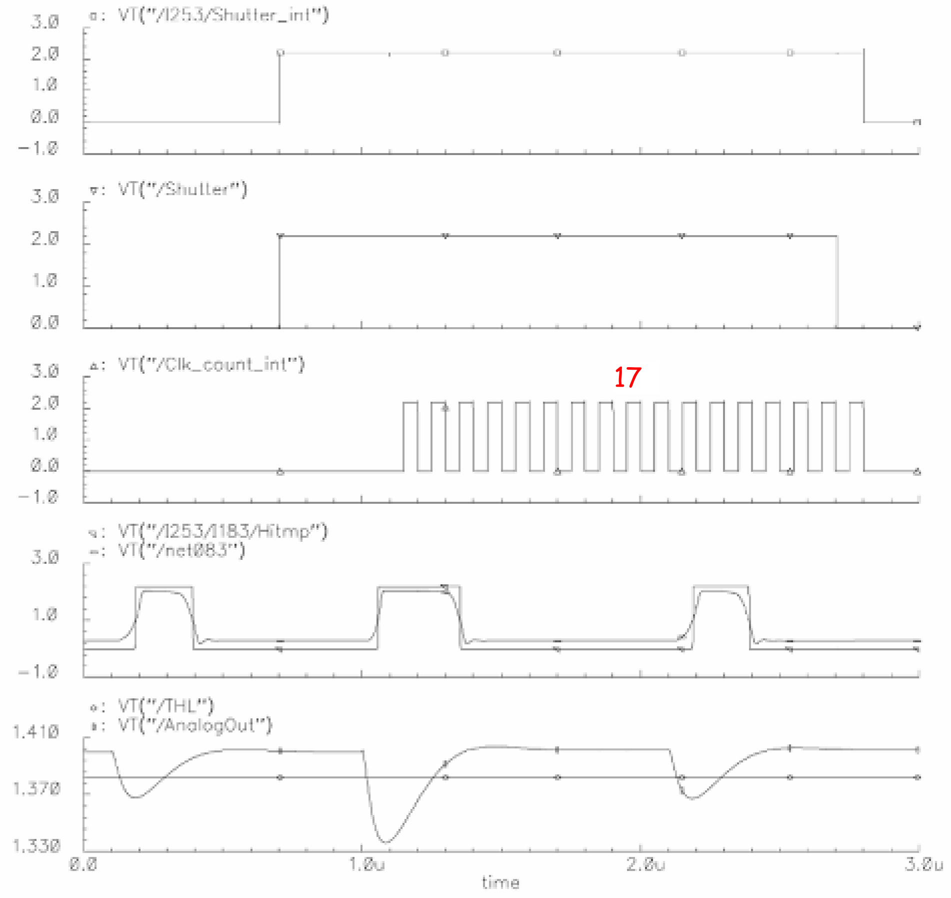
All these values are extracted from simulations !!!

Timepix Synchronization Logic control

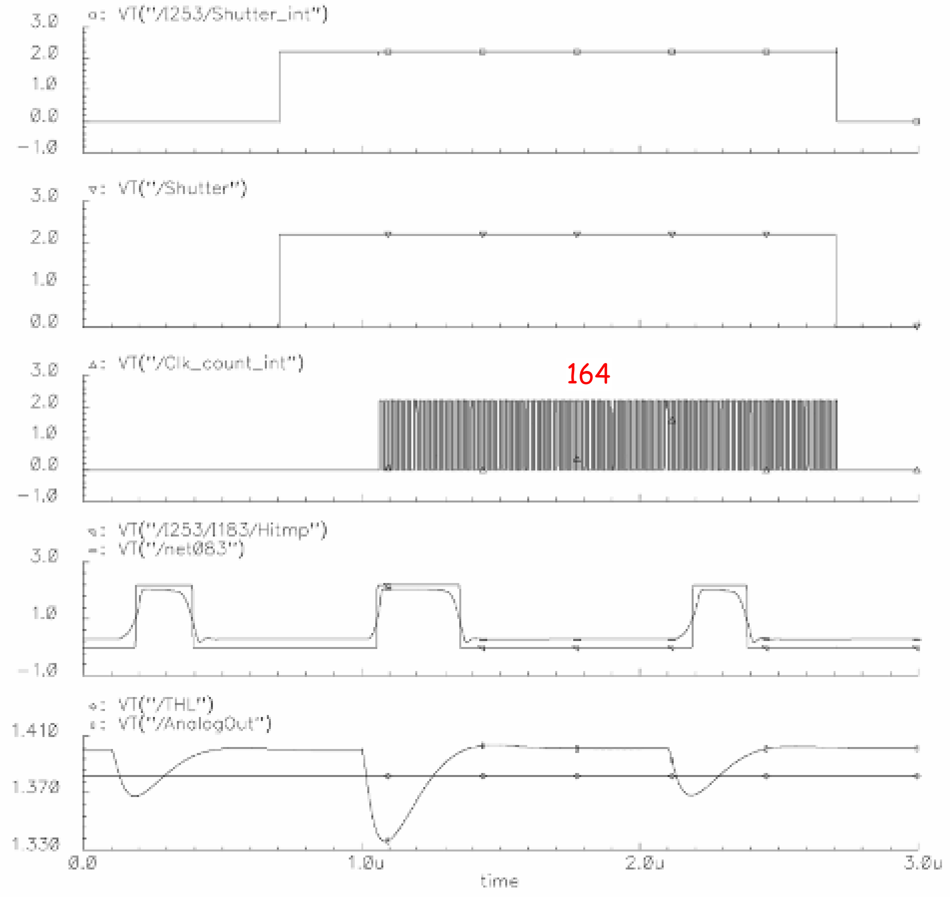
- Use of 3-bit High threshold adjustment bits for : 4th equalization bit and P0, P1.
- Each pixel can be configured independently in 5 different modes.
- This logic needs 128 Trts (Mpix2MXR20 had 92 Trts)
- Logic consumes power only when a hit is present

Mask	P1	P0	Mode
0	0	0	Masked
0	0	1	Masked
0	1	0	Masked
0	1	1	Masked
1	0	0	Medipix
1	0	1	TOT
1	1	0	Timepix-1hit
1	1	1	Timepix

Timepix Mode (P0=1,P1=1)

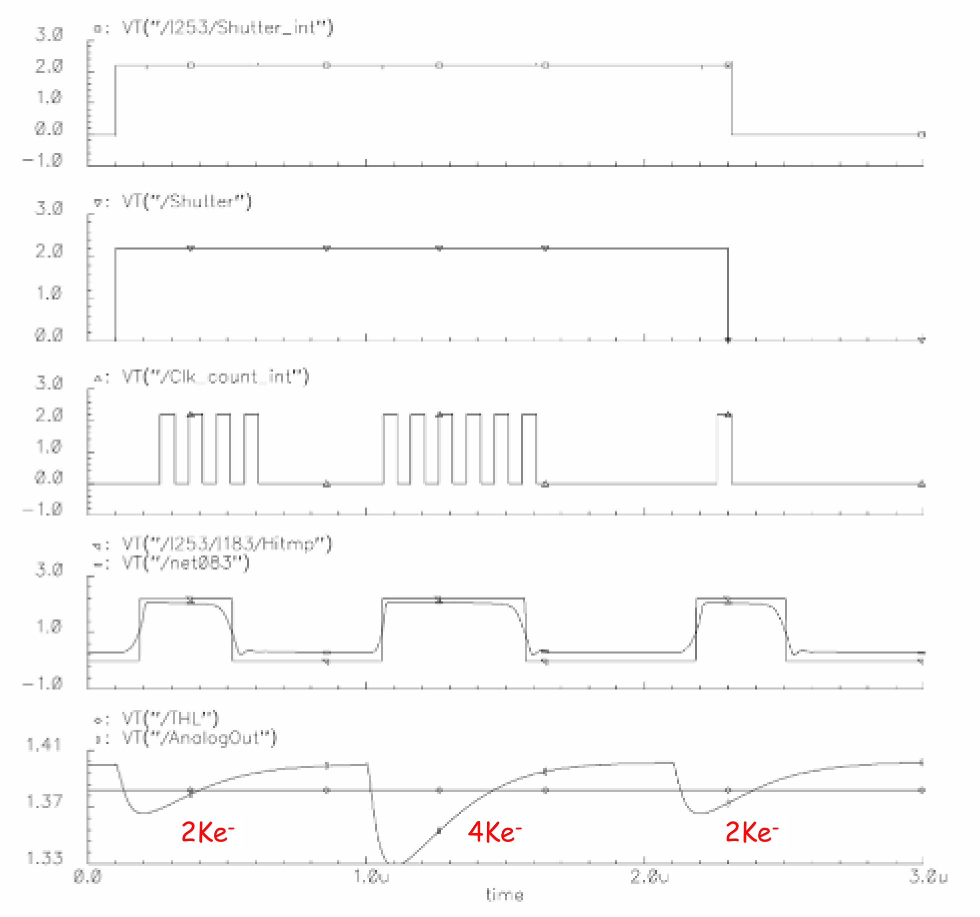


10MHz

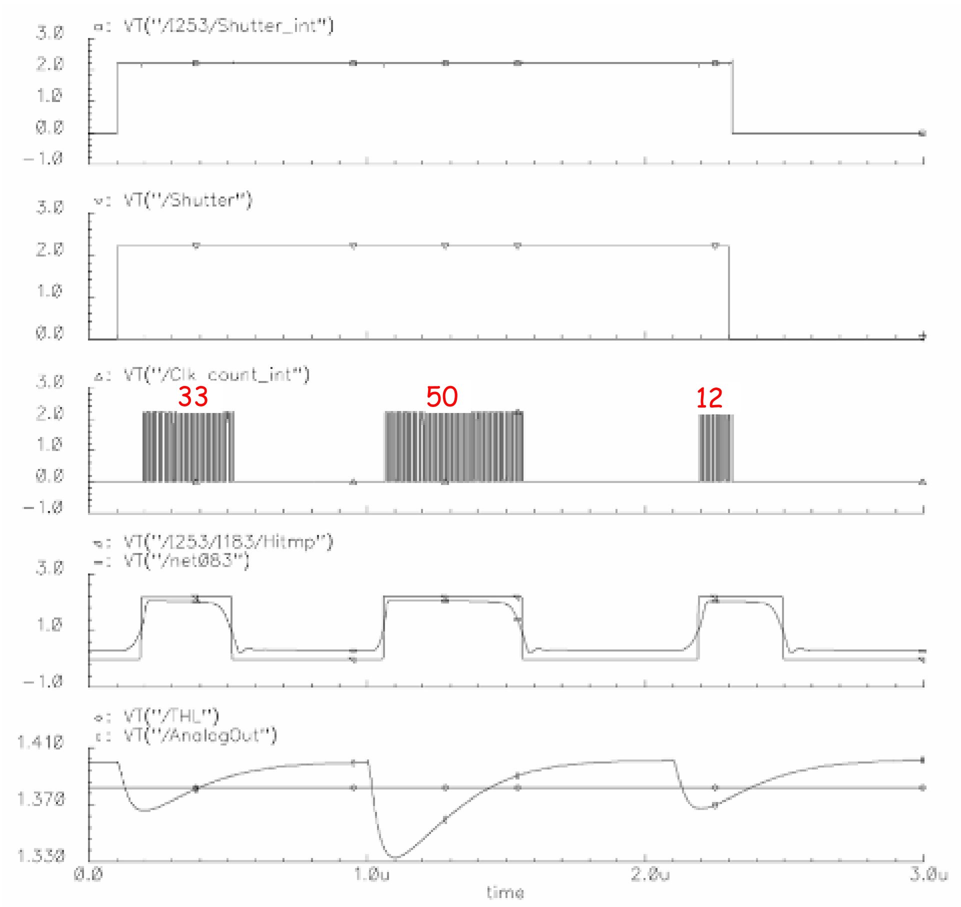


100MHz

TOT Mode (P0=1,P1=0)

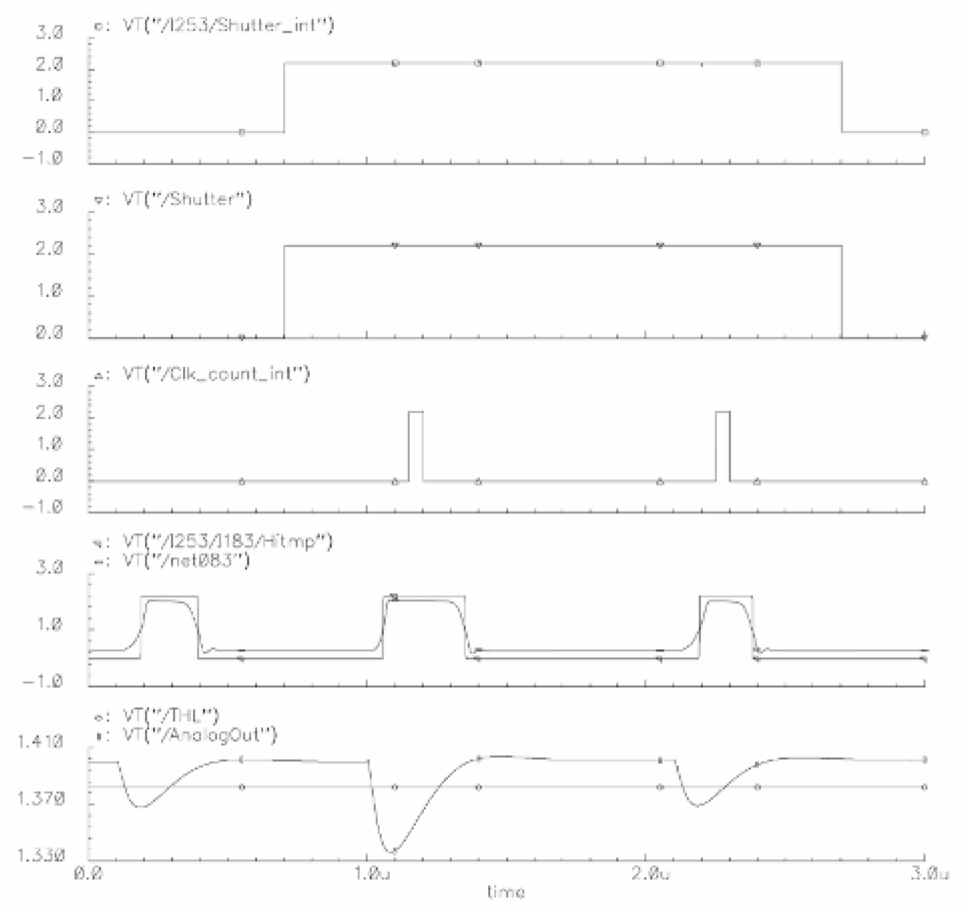


10MHz

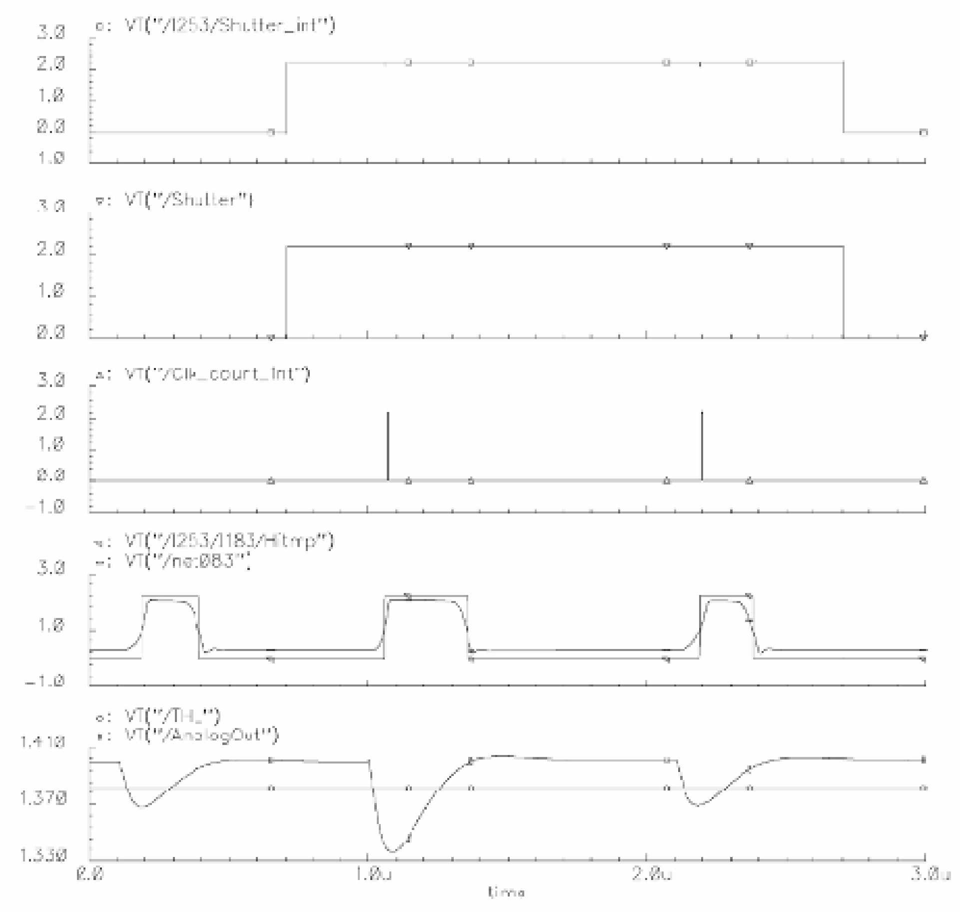


100MHz

Medipix Mode (P0=0,P1=0)

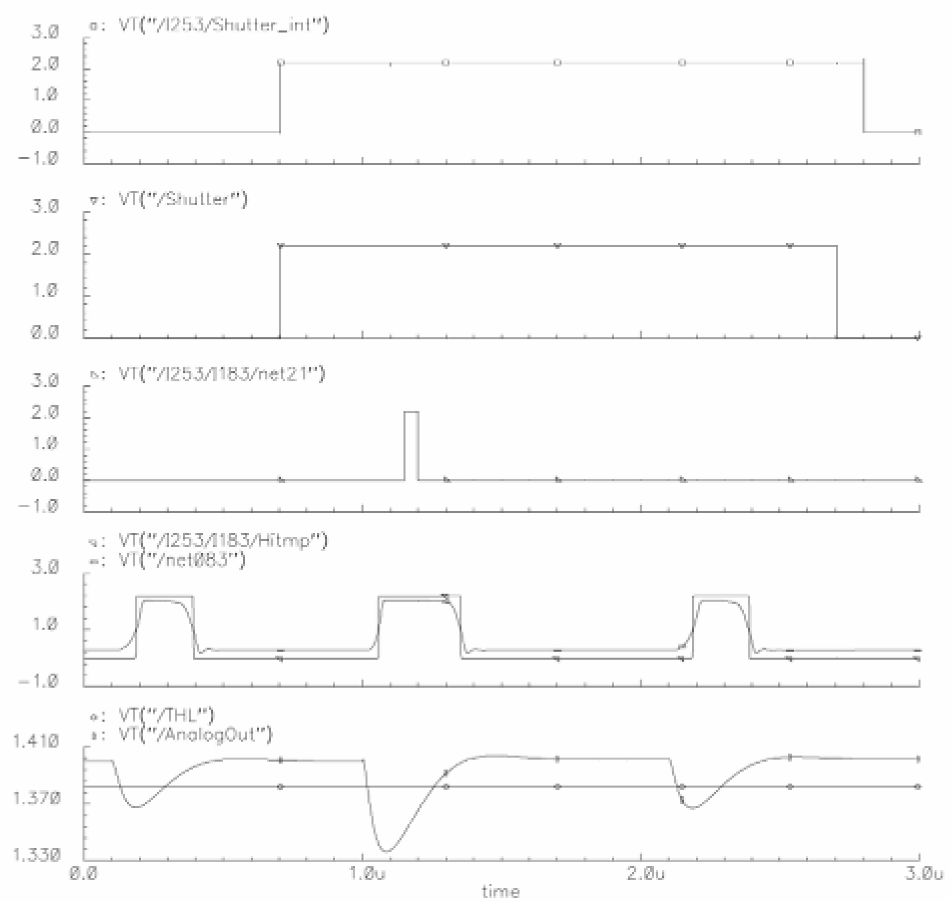


10MHz

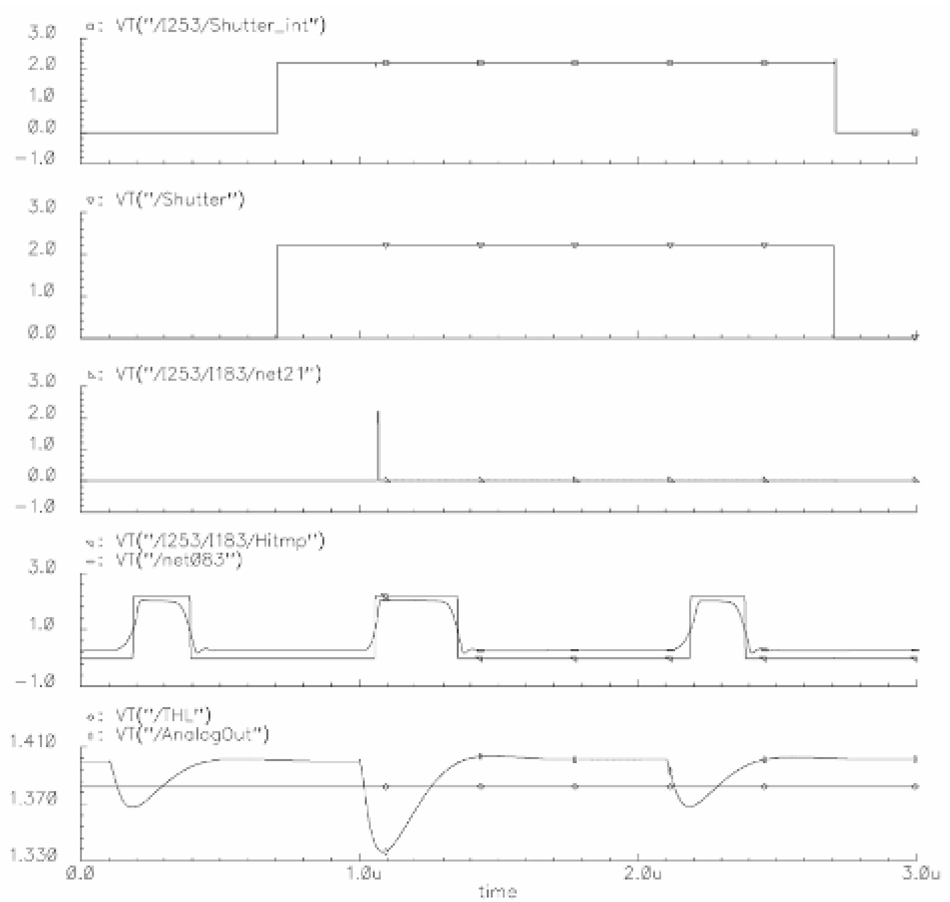


100MHz

Timepix-1h Mode (P0=0,P1=1)

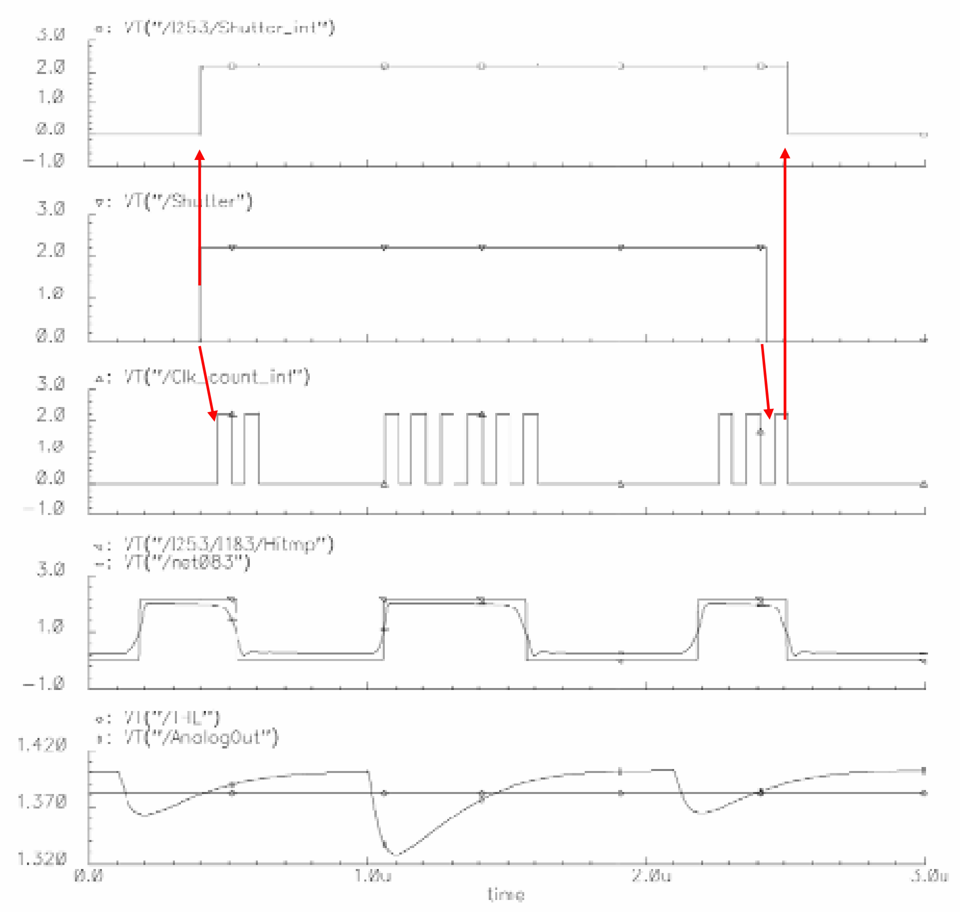


10MHz



100MHz

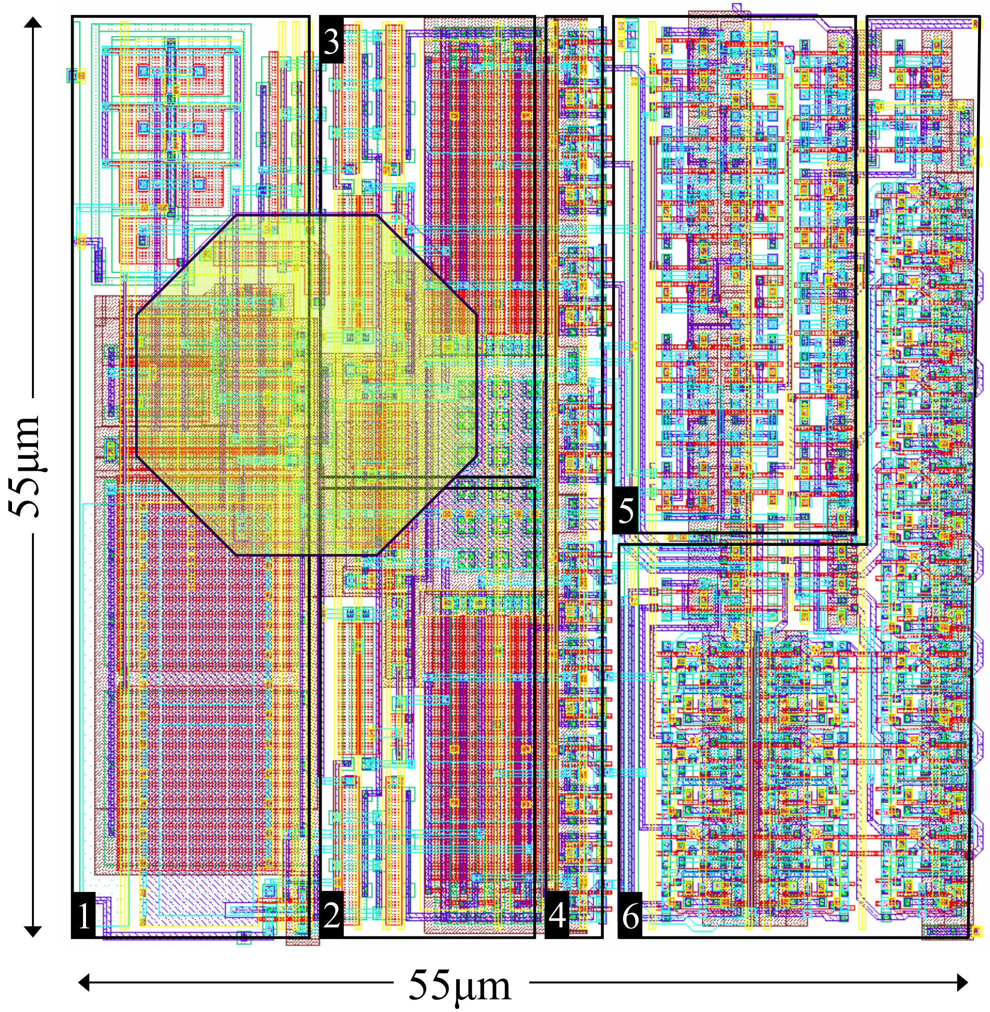
TOT Mode (P0=1,P1=0)



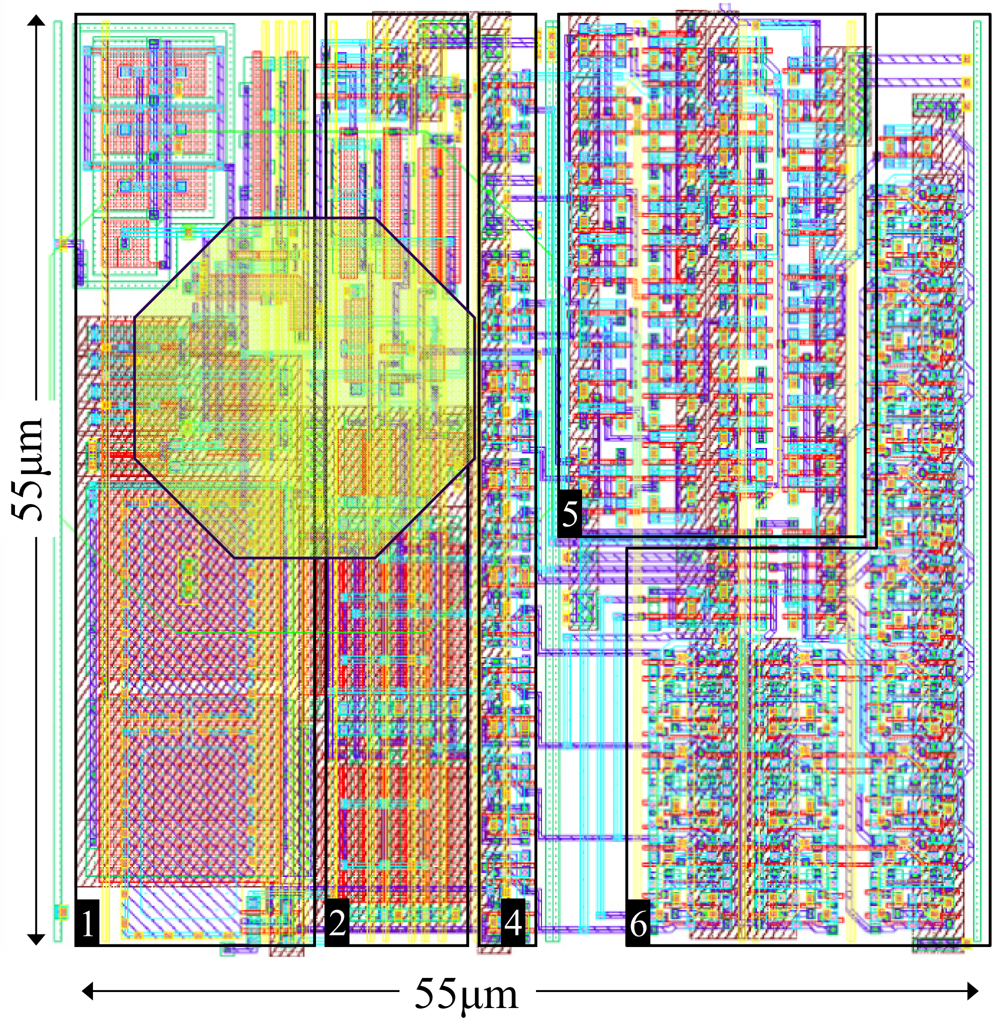
- Internal Shutter is always synchronous to the clock to avoid glitches
- Counter starts counting if a hit is present when shutter starts
- Shutter closing happens with a maximum delay of 1Tclk if a hit is present when shutter closes

Timepix Layout status (2/5/06)

Mpix2MXR20 layout



Timepix layout

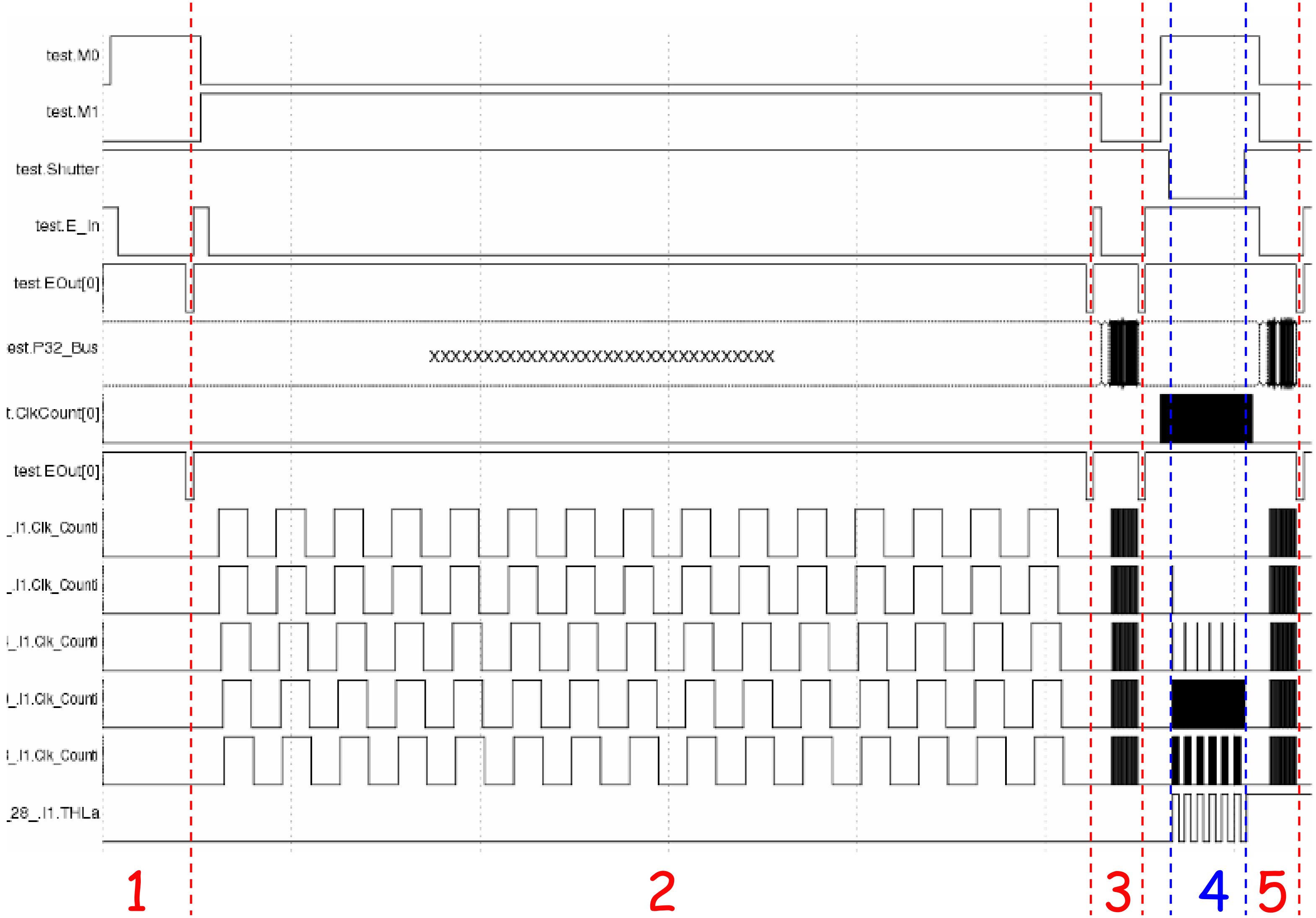


Periphery Verilog Simulations

- This simulation tests 1 row of pixels and the full chip control logic
- Tested with normal and corner ($\pm 3\sigma$) parameters successfully
- Pixel control logic is initialized after a set mask command
- M0=1 and M1=1 when counting will enable the clock distribution to the pixel matrix

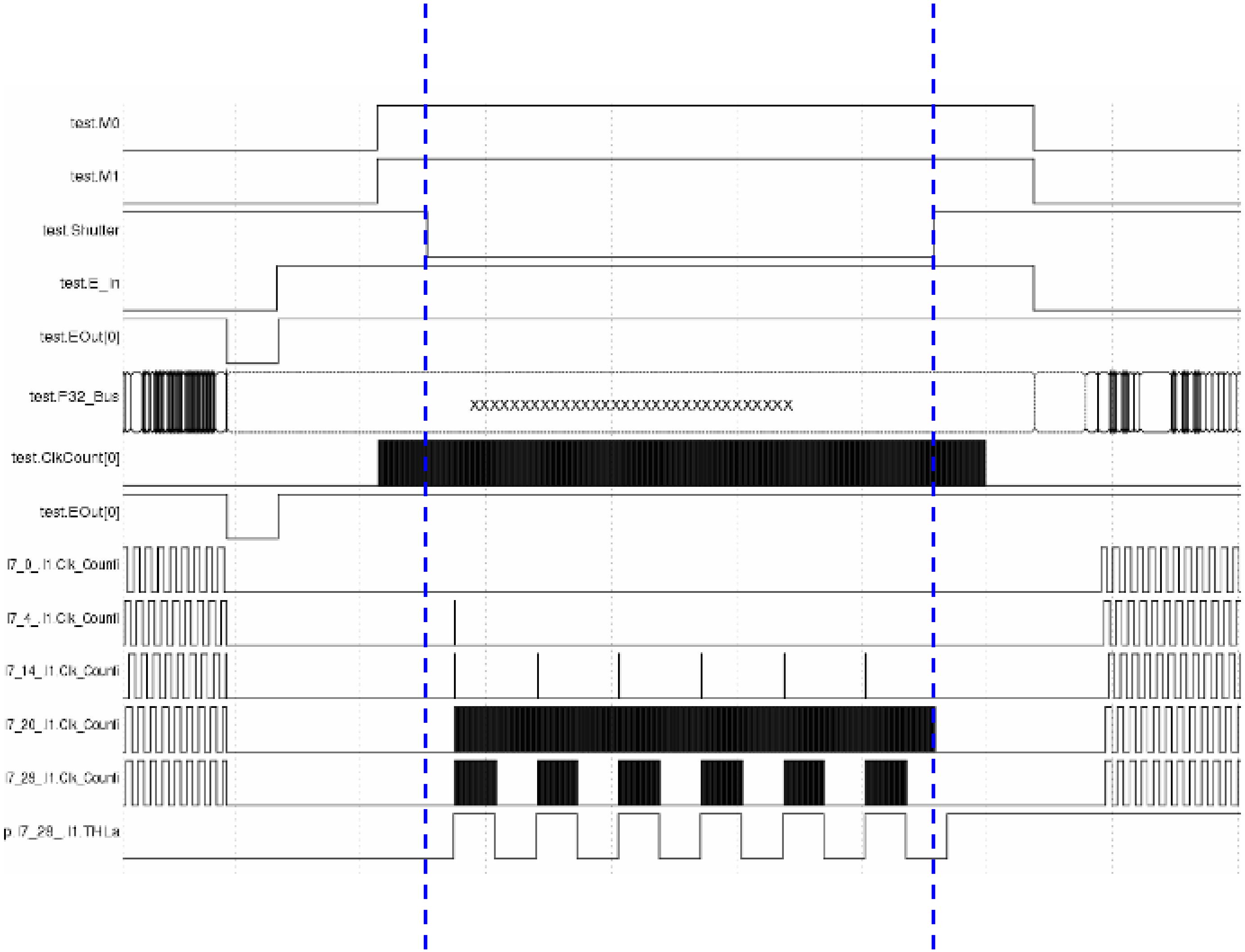
M0	M1	Enable_IN	Shutter	Reset	P_S	I/O	FClock num (per chip)	Operation
X	X	X	X	0	X	I	X	**General reset of the chip**
1	1	X	0	1	X	X	X	**Counting**
0	0	0	1	1	0	I/O	917768	**Serial Readout Matrix (Slow Reset Matrix)**
0	0	0	1	1	1	I/O	28688	**Parallel Readout Matrix (Fast Reset Matrix)**
0	1	0	1	1	X	I	917768	**Set Matrix**
1	0	0	1	1	X	I/O	264	**Write/Read FSR (DACs and CTPR)**

Single chip Verilog simulation



1:SetDACs
2:SetMatrix
3:ResetMatrix (PS=1)
4:Counting
5:Readout (PS=1)

Counting Modes (Mask,P0 and P1)



⇐ Pixel Masked P0=X, P1=X and Mask=1

⇐ Tpix-1h mode P0=0, P1=1 and Mask=0

⇐ Mpix2 mode P0=0, P1=0 and Mask=0

⇐ Tpix mode P0=1, P1=1 and Mask=0

⇐ CCD mode P0=1, P1=0 and Mask=0

Medipix2 vs Timepix

	Medipix2	Timepix
Physical dimensions	=	=
IO PADs	=	=
Charge collection	e^-, h^+	e^-, h^+
Pixel functionality	PhotonCounting	PhotonCounting, TOT, Timepix
Amplifier Gain	~10mV/Ke^-	~18mV/Ke^-
Noise	~110e^-	~75e^-
Linearity	Up to 100Ke^-	Up to 50Ke^-
Thresholds	2 (3+3 bits adj)	1 (4bits adj)
σ equalized	~100e^-	~25e^-
Minimum Threshold	~900e^- (measured)	~500e^- (expected)*
Counter Depth/Overflow	14-bits/Yes	14-bits/Yes
Max Analog power	10μW/pix 300mA/chip	6.5μW/pix 190mA/chip
***Static* Digital Power**	none	200mA@100MHz
Readout	Serial/Parallel	Serial/Parallel
Readout compatibility	100%	95% (Clock active when shutter ON)

Summary

- Medipix2 chip has shown potential for a *silicon TPC* with 2 different gas gain grids
- To exploit the 3D (position + time) a clock stamp up to 100 MHz has to be added
- Other projects will also profit the TOT mode added to this chip
- Expected submission by the end of June2006