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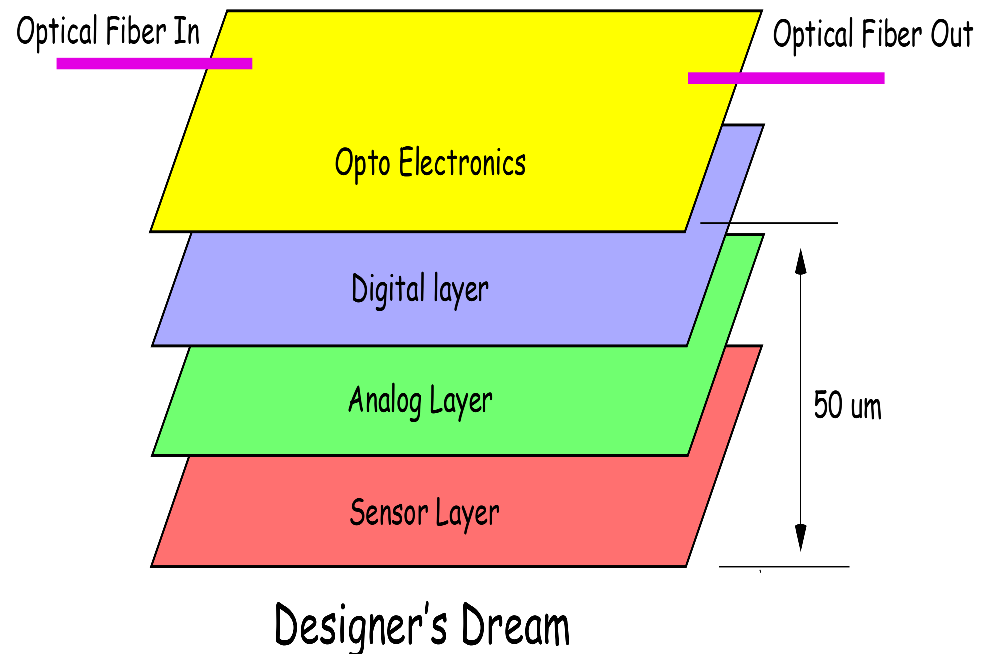
Introduction

- 3D integrated circuits is becoming a topic of interest in many technical journals and conferences. [1,2] (Note: As you will see, this is different than 3D detectors often described in the HEP literature.)
- This work can provide new opportunities for us to explore issues such as:
  - Low mass
  - High density
  - Increased functionality
- This talk will present
  - An overview of 3D IC principles
  - Three examples of 3D ICs
  - A design showing a 3D circuit for HEP

What is a 3D Integrated Circuit?

- A 3D chip is comprised or 2 or more layers of semiconductor devices which have been thinned, bonded together, and interconnected to form a “monolithic” circuit.
- Frequently, the layers (also called tiers) are comprised of devices made in different technologies.



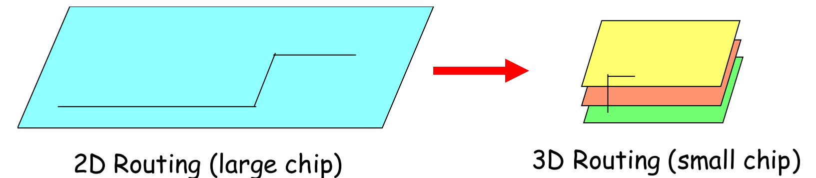
Designer's Dream

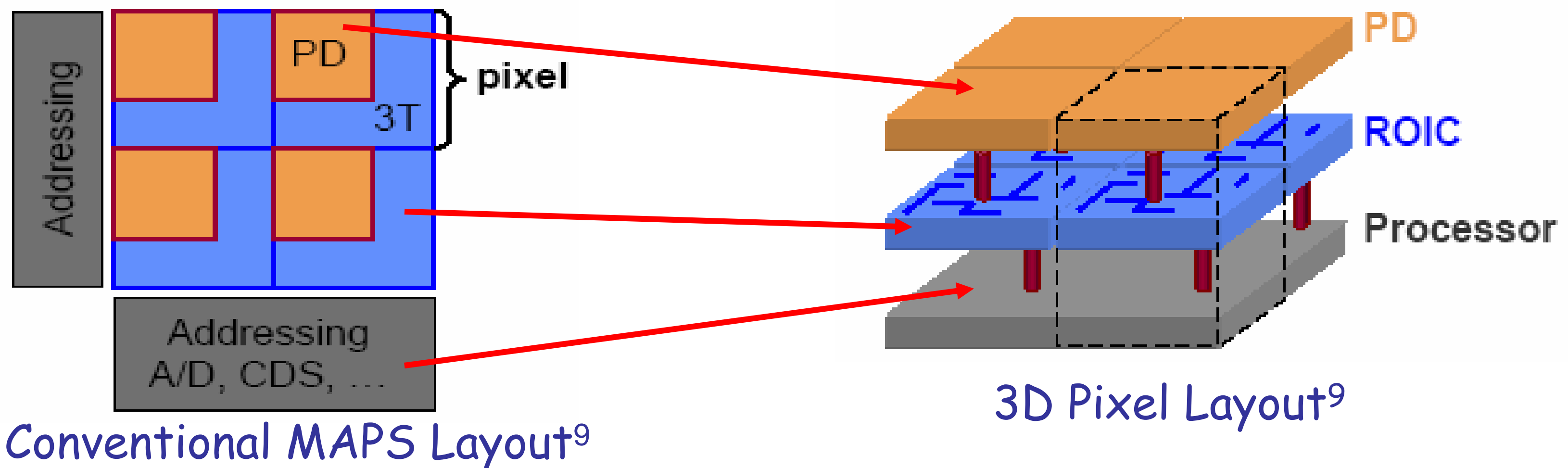
Why Consider 3D Now?

- The move to 3D is being driven entirely by industry needs.
  - In submicron processes, RC delay is a limiting factor in performance improvement.
  - Low k dielectrics to reduce C have been difficult to implement.
  - Circuit overhead is taking a larger fraction of the chip area.
- 3D is discussed in the ITRS (International Technology Roadmap for Semiconductors) as an approach to improve circuit performance and permit continuation of Moore's Law.

What are the Advantages?

- Going 3D reduces trace length
  - Reduces R, L, C
  - Improves speed
  - Reduces interconnect power, crosstalk
- Reduces chip size
- Processing for each layer can be optimized
- MAPS as an example
  - 100% diode fill factor
  - Four-side abuttable devices



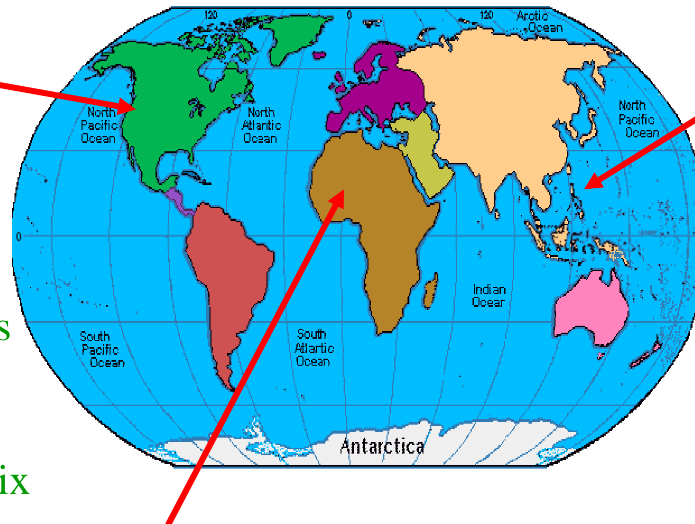


Conventional MAPS Layout[9]

3D Pixel Layout[9]

Who is Working on 3D ICs?

USA:
Albany Nanocenter
U. Of Kansas,
U of Arkansas
Lincoln Labs, AT&T
MIT,RPI, RTI, TI
IBM, Intel, Irvine Sensors
Micron, Sandia Labs
Tessera, Tezzaron,
Vertical Circuits, Ziptronix

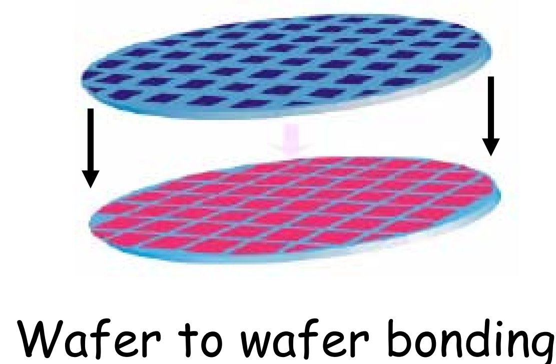


Asia:
ASET, NEC, University of Tokyo,
Tohoku University, CREST,
Fujitsu, ZyCube, Sanyo,
Toshiba, Denso, Mitsubishi, Sharp,
Hitachi, Matsushita, Samsung

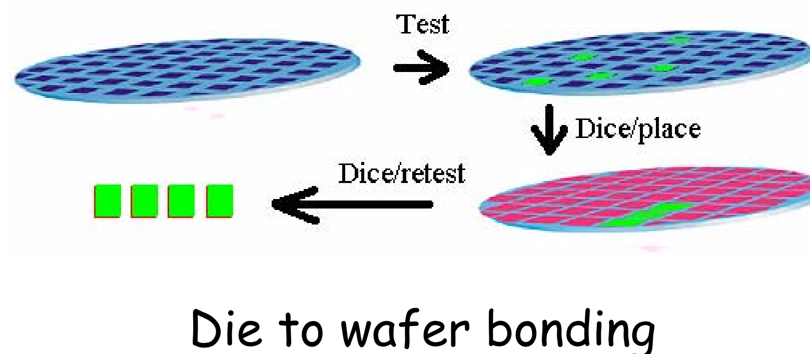
Europe: Fraunhofer IZM, IMEC Delft,
Infineon, Phillips, Thales, Alcatel Espace,
NMRC, CEA-LETI, EPFL, TU Berlin

Groups are Pursuing Different Options

- The different organizations are taking many different approaches to 3D fabrication.[3]
- The approaches can be divided into 2 general categories:
  - Wafer to wafer bonding
  - Die to wafer bonding



Wafer to wafer bonding



Die to wafer bonding

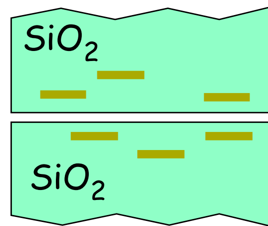
Advantages and Disadvantages

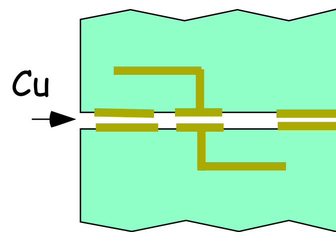
- Wafer to wafer bonding approach
  - Advantages
    - All work generally handled by one fabricator
    - Thinner tiers with shorter vias are possible
  - Disadvantages
    - Dies must be same size
    - Precise alignment across wafer is essential.
    - Yield is reduced with the number of layers.
- Die to wafer bonding approach
  - Advantages
    - Different vendors can be used for different tiers
    - Known good die can be used to improve yield
  - Disadvantages
    - More handling of individual parts

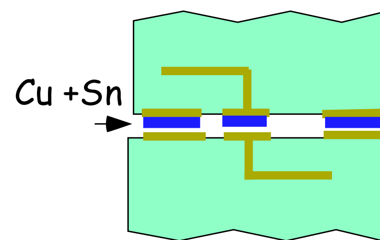
Four Key Technologies for 3D ICs [4]

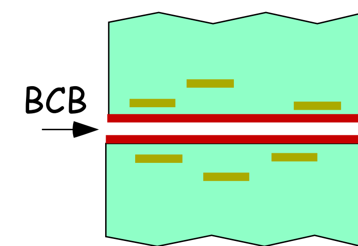
- Bonding between layers
  - Oxide to oxide fusion
  - Direct copper fusion
  - Copper/tin bonding
  - Polymer bonding
- Wafer thinning
  - Grinding, lapping, etching, and CMP
- Through wafer via formation and metallization
  - With isolation
  - Without isolation
- High precision alignment
  - Less than 1 micron

Bonding Techniques









Direct silicon fusion bonding

Mechanical bond

Exceptionally flat and clean surfaces are necessary.

Pressure and temperature used to fuse wafers.

Plasma treated surfaces reduce bonding temperature to 300 ^{0}C.

Copper to copper fusion bonding

Electrical + mech.

Very high degree of planarity is needed.

Full contact is necessary

Large area of copper generally used to mate surfaces.

Bonding done at 400 ^{0}C

Copper-tin eutectic bonding

Electrical + mech.

Tin is added to form eutectic bond at a lower temperature (250 ^{0}C).

Large area of copper generally used.

Can be used to encapsulate bonds.

Adhesive (BCB) bonding

Mechanical bond

Typical adhesive polymer used is BCB.

Most tolerant of uneven bonding surfaces such as non-planarized surfaces.

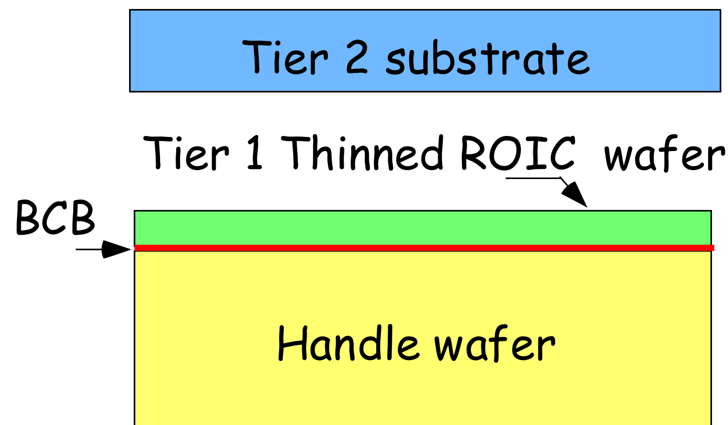
Low adhesive temperature may affect later procesing steps.

Wafer Thinning

- Depending on the approach used, thinning of individual tiers may be done before or after bonding to another tier.
- Thinning is generally done by grinding and lapping followed by etching (plasma or wet) and CMP (chemical mechanical polishing)
- Wafers are routinely thinned to 50 μm in production and thinning to 6 μm has been done.
- Several articles have been published showing little or no degradation of parts thinned to 12 to 25 μm. [5,6]
- At Fermilab we are presently thinning FPIX2 parts to various thicknesses down to 15 μm to study performance issues.

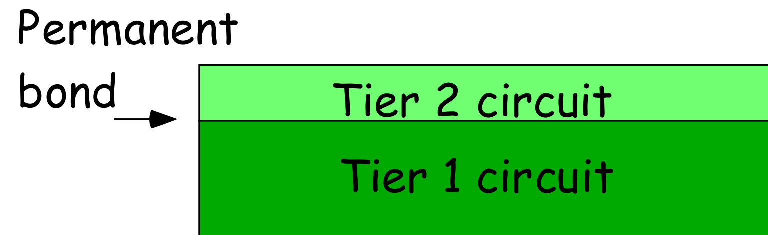
Thinning Approaches

Thinning before bonding tiers



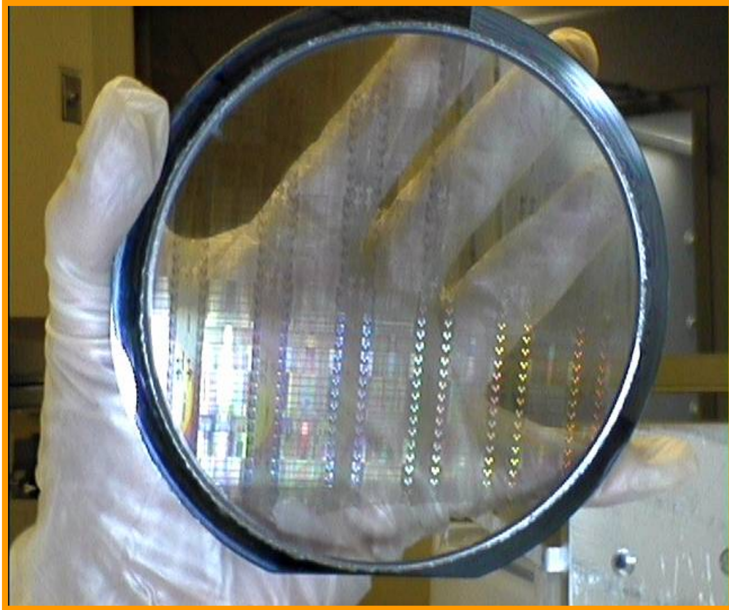
Mount Tier 1 ROIC wafer on handle wafer using BCB, thin to desired thickness. Mount thinned ROIC wafer to tier 2 substrate and remove handle wafer.

Thinning after bonding tiers



After bonding tier 2 to tier 1, tier 2 is thinned to the desired thickness before further processing

Thinned Wafers



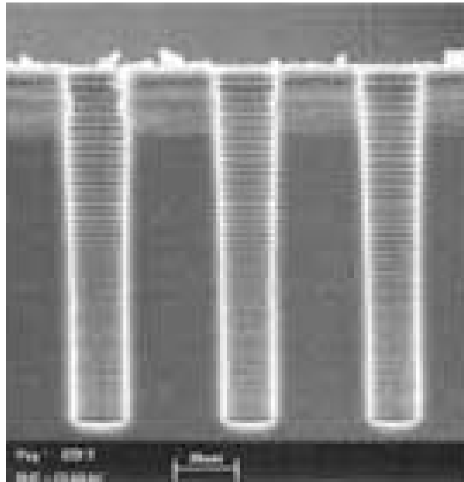
Thinned wafer mounted on Quartz handle wafer (MIT Lincoln Labs)

Wafer thinned to 50 microns (leti)

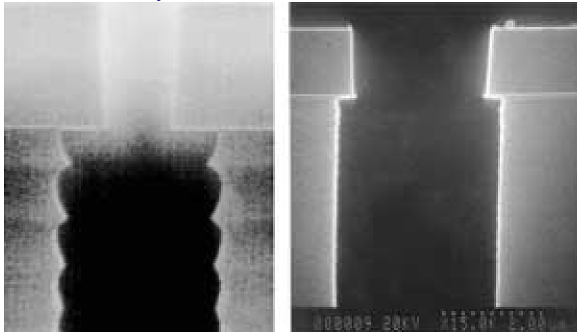
Wafer Via Formation

- Two different techniques are used for via formation depending on the type of the substrate.
  - For vias in silicon (CMOS), the Bosch process (SF_6) is used to etch very deep vias (up to 400 um) with nearly vertical side walls. [7]
  - For vias in oxide (SOI), a standard plasma etching process is used, resulting in tapered side walls
- Isolation
  - In CMOS wafers, the via walls must be insulated (C_4F_8) before filling with metal
  - In SOI wafers, no passivation is necessary (advantage for SOI)
- Vias are filled TiN/Cu or tungsten
- Vias as small as 1.5 um have been made

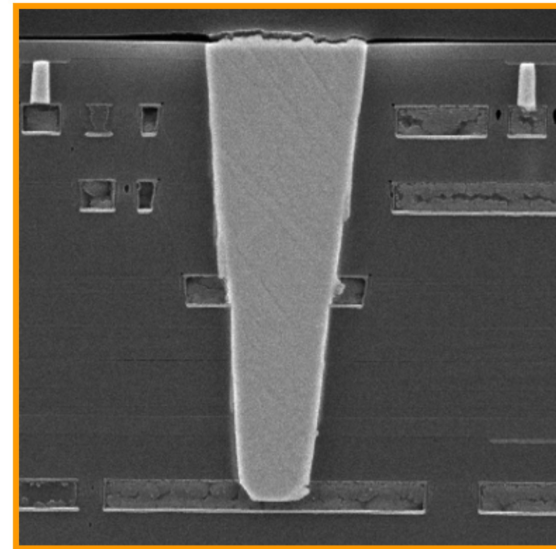
Via Formation



SEM of 3 vias made with Bosch process [7]



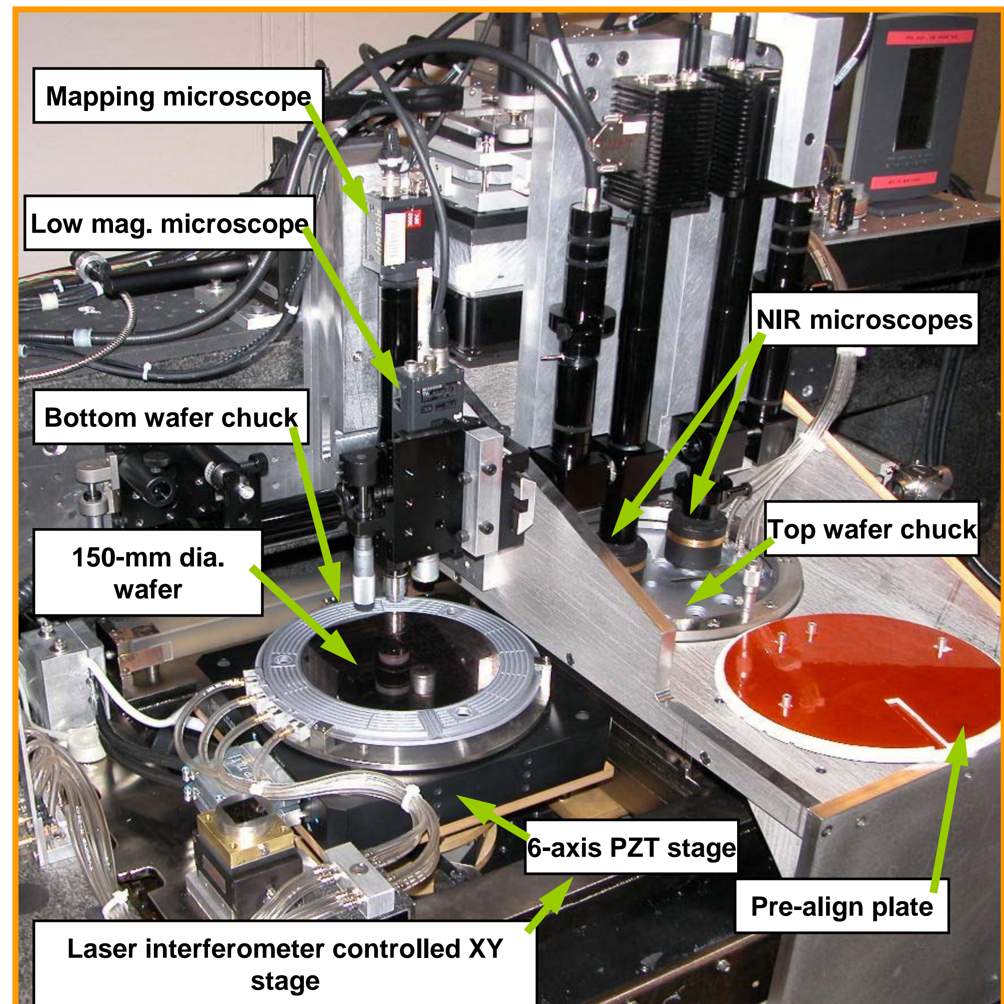
Close-up of walls with/without Scallops in Bosch process [7]



Tapered wall using high density plasma oxide etch (MIT Lincoln Labs)

Alignment

- Need wafer-to-wafer alignment accuracy compatible with a submicron 3D Via
- Tools used based on modern IC wafer stepper technology
- 0.5 μm 3-sigma overlay demonstrated at MIT LL.

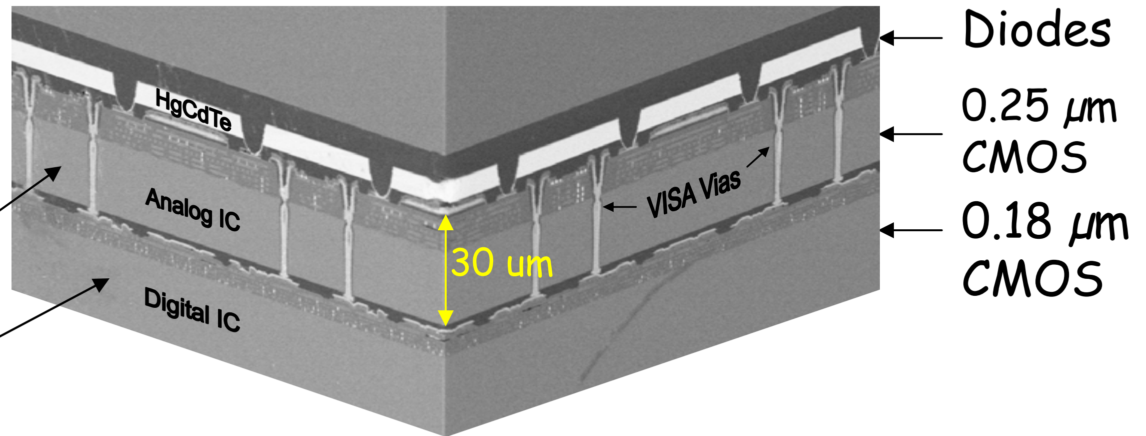


3D Projects of Interest to HEP

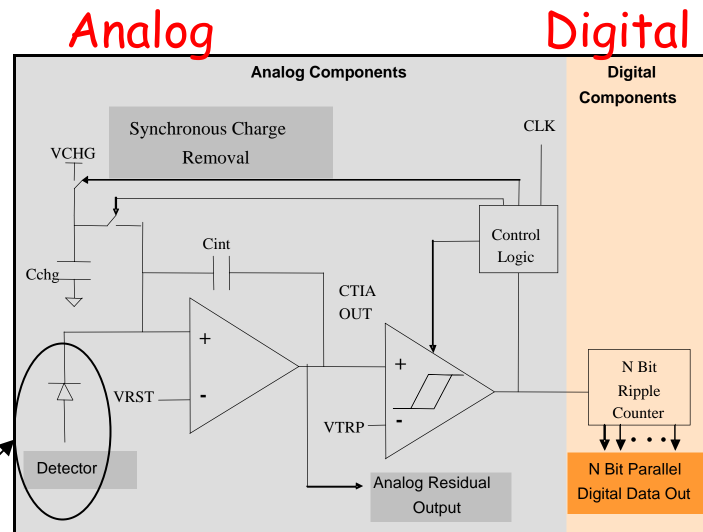
- RTI International and DRS Technologies
  - Example 1: 3D Infrared Focal Plane Array [8]
    - 30 μm pixels
    - 3 tiers of electronics
- MIT LL
  - Example 2: Megapixel CMOS Imager Fabricated in Three Dimensional Integrated Circuit [9]
    - 8 μm pixels
    - 3 tiers of electronics
  - Example 3: Laser Radar Imager based on 3D Integration of Geiger Mode Avalanche Photodiodes with Two SOI Timing Circuit Layers. [10]
    - 30 μm pixels
    - 3 tiers of electronics

3D Infrared Focal Plane Array

- 256 x 256 array with 30 μm pixels
- 3 Tiers
  - HgCdTe (sensor)
  - 0.25 μm CMOS (analog)
  - 0.18 μm CMOS (digital)
- Die to wafer stacking
- Polymer adhesive bonding
- Bosch process vias (4 μm) with insulated side walls
- 99.98% good pixels
- High diode fill factor



Array cross section

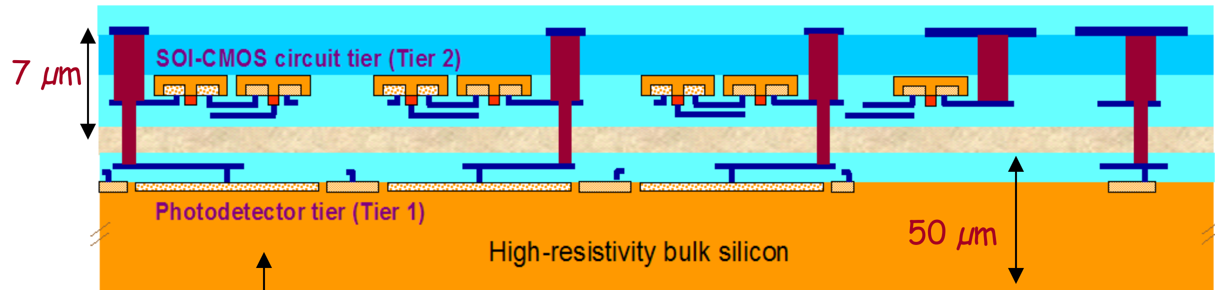


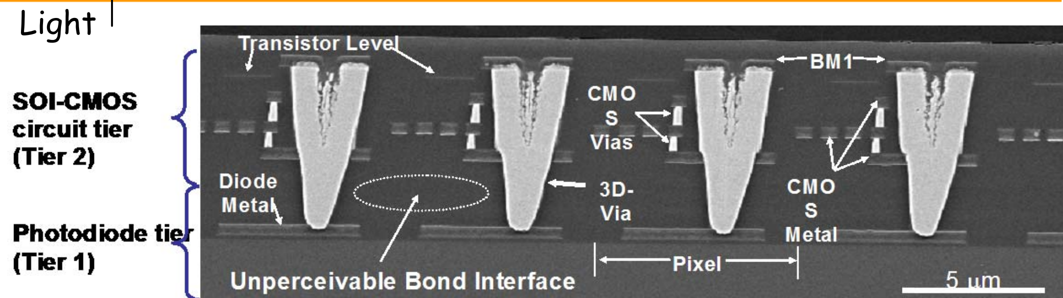
3 Tier circuit diagram

Infrared image

3D Megapixel CMOS Image Sensor

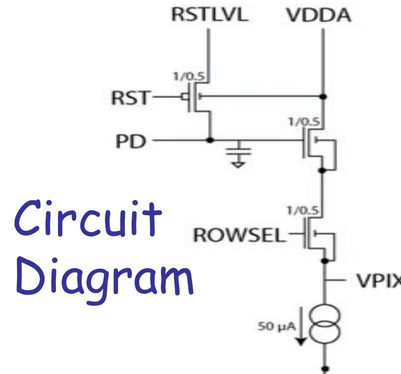
- 1024 x 1024, 8 μm pixels
- 2 tiers
- Wafer to wafer stacking (150 mm to 150 mm)
- 100% diode fill factor
- Tier 1 - p^+n diodes in >3000 ohm-cm, n-type sub, 50 μm thick
- Tier 2 – 0.35 um SOI CMOS, 7 μm thick
- 2 μm square vias, dry etch, Ti/TiN liner with W plugs
- Oxide-oxide bonding
- 1 million 3D vias
- Pixel operability >99.999%
- 4 side abuttable array





Drawing and SEM Cross section

Circuit Diagram



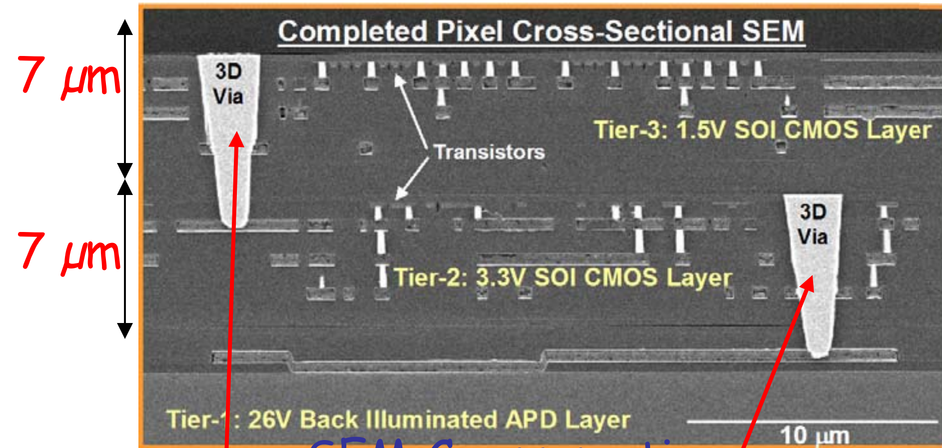
Image

3D Laser Radar Imager

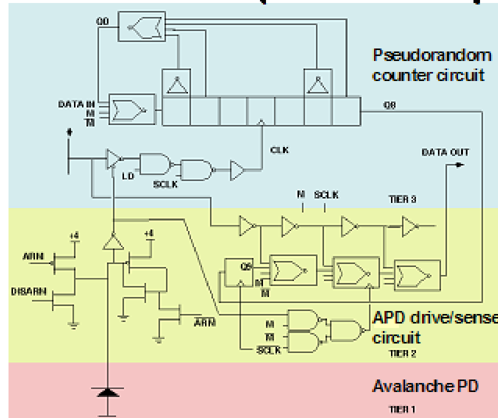
- 64 x 64 array, 30 μm pixels
- 3 tiers
  - 0.18μm SOI
  - 0.35 μm SOI
  - High resistivity substrate diodes
- Oxide to oxide wafer bonding
- 1.5 μm vias, dry etch
- Six 3D vias per pixel

7 μm

7 μm



SEM Cross section

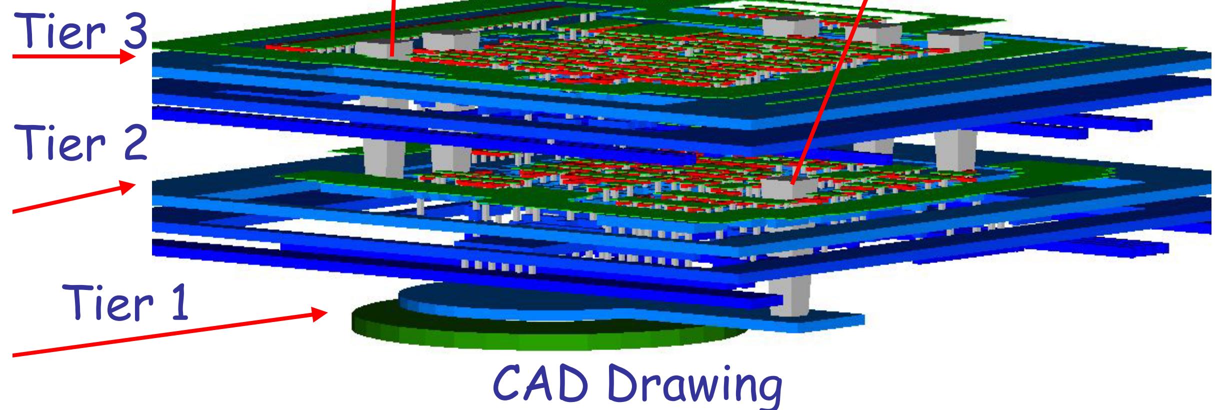


Schematic

Tier 3

Tier 2

Tier 1



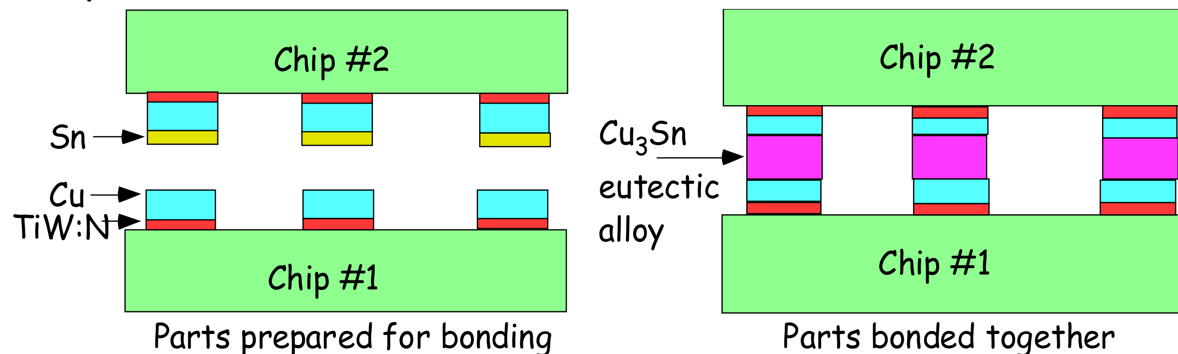
CAD Drawing

Two Projects Using 3D Concepts at Fermilab

- Investigate 3D thinning and bonding techniques with existing CMOS devices
  - BTEV pixel (FPIX) readout chips
  - BTEV pixel detectors
- Participate in 3 tier multi-project run
  - Design prototype pixel array with full readout for ILC

1) Study 3D Processes with Existing Wafers

- Thin pixel ROIC (50 x 400 um pixels) as small as possible (down to 15 um) and study performance. (parts have been thinned, testing to begin soon).
- Add Cu/Sn to ROIC pads and Cu to detector pads.
- Perform die to wafer bonding.
- Evaluate eutectic bonding technique
  - Can be used for face to face or face to back connections.
  - Face to face bonding could be fine pitch (15 um) alternative to bump bonding.
- Issues
  - Cu generally covers large fraction of mating surface area.
  - The Cu bond is typically 10 um thick which is about 0.07% of X_0.
  - Study reduction of copper coverage to less than 10% of surface area.
- Process used by IZM, RTI, and others



2) Design of Pixel Readout Chip for ILC

- ILC Maximum hit occupancy
  - Assumed to be 0.03 particles/crossing/mm^2
  - Assume 3 hits pixels/particle (obviously this depends somewhat on pixel size and charge spreading)
  - Hit rate = 0.03 part./bco/mm^2 x 3 hits/part. x 2820 bco/train = 252 hits/train/mm^2. [11]
- Propose digital read out approach
  - Want better than 5 μm resolution
  - A square 15μm cell gives 15/3.46 = 4.3 μm.

Sparsification and Time Stamping

- Sparsification is highly desirable to reduce the volume of data being transmitted off any chip and to reduce the digital power dissipated in the chip.
- Although the occupancy is relatively low, Time Stamping is necessary to define when a hit in a given area occurred in order to reconstruct a hit pattern in association with data from other detectors.

Required Pipeline Depth

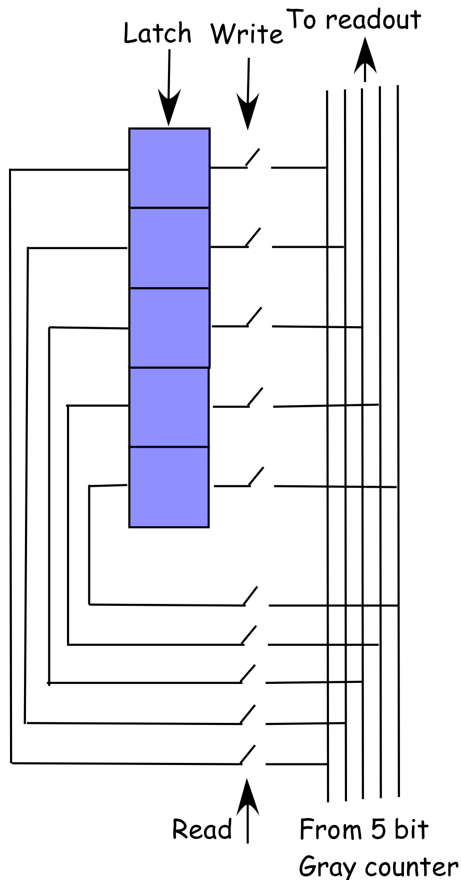
- Occupancy for single 15 μm x 15 μm pixel
  - Occupancy = 250 hits/mm^2 (15μm x 15μm)
    = 0.056 hits/bunch train
  - Chance of a single cell being hit twice in a bunch train = .056 x .056 = .0031 = 0.3%
  - Therefore, with a depth of only one, 99.7% of hits are recorded unambiguously.
- For comparison, occupancy in a 4 x4 array of 15 um pixels would require a 3 deep time stamp buffer and provide 98.6% efficiency.

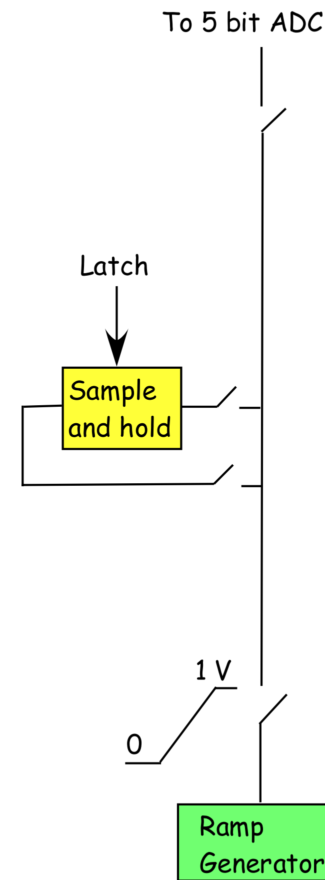
Chip Design Choices

- Use token passing scheme developed for BTEV pixel and silicon strip RO chips to sparsify data output.
- Divide the bunch train into 32 time slices. Each pixel stores one time stamp equivalent to 5 bits of time information.
- Do not store pixel addresses in the pixel cell.
- Store the time stamp in the hit pixel cell.
- Minimize number of transistors/pixel as much as possible.
- For time being, consider independent pixel cell processing. Multiple cell processing (cell grouping) on multiple tiers could reduce the overall transistor count.

Pixel Time Stamping

Various MAPS schemes for ILC have suggested 20 time stamps to separate hits in the 2820 bunch train.
Proposed 3D scheme using 32 time stamps.





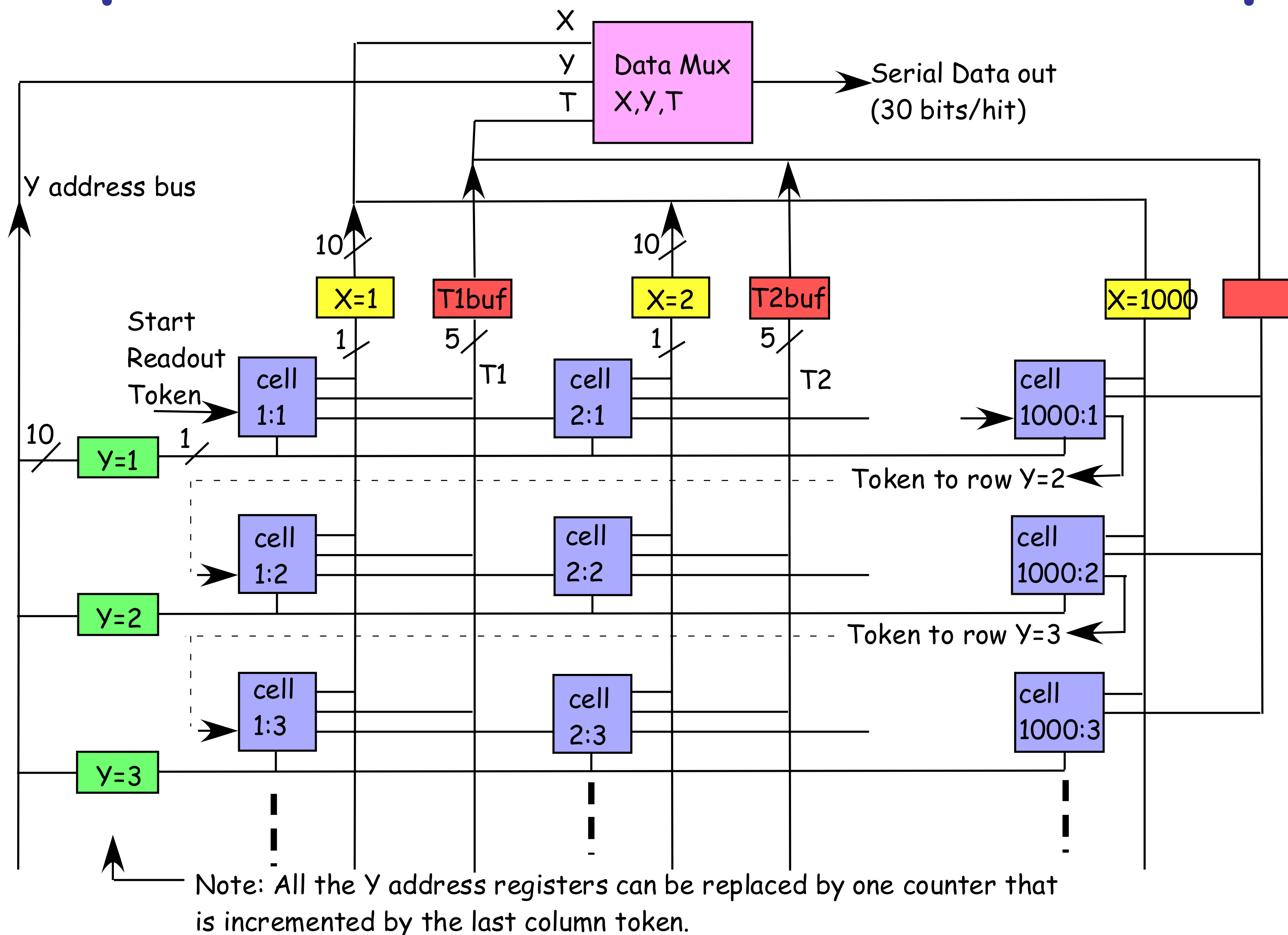
Counter operates at a slow speed, 32 KHz, (30 usec/step)

All digital - 10 transistors/bit

Ramp operates at low speed for low power. ADC accuracy may be an issue

Analog approach - fewer transistors

Sparsified Readout Concept



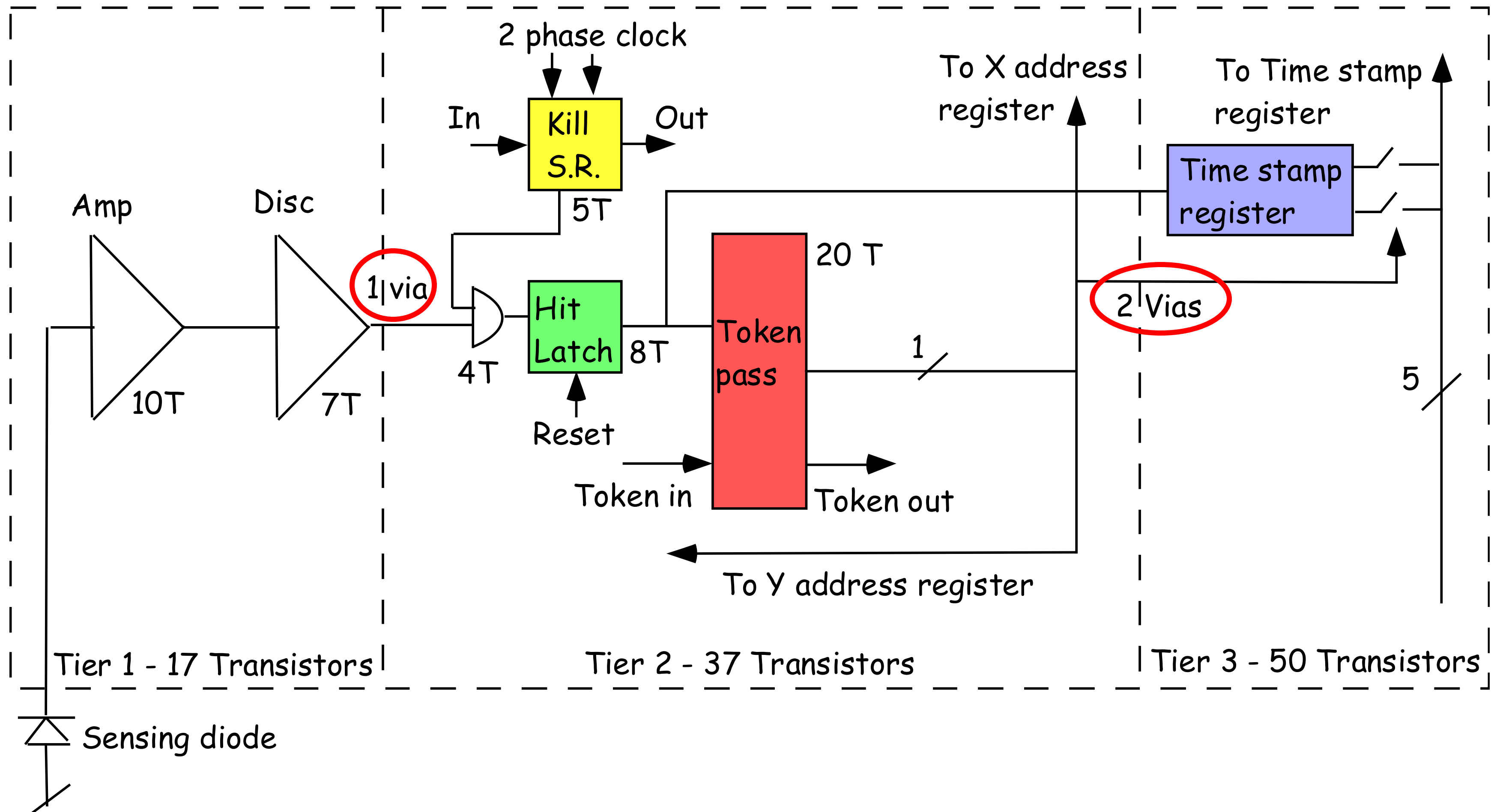
Sparsified Readout

- During acquisition, a hit sets a latch.
- Sparse readout performed row by row.
- To start readout, all hit pixels are disabled except the first hit pixel in the readout scan.
- The pixel being read points to the X address and Y address stored on the perimeter and at the same time outputs the Time Stamp information from the pixel.
- While reading out first address and time stamp, a token scans ahead looking for next pixel to readout.
- Chip set to always readout all pixels with X=1 address and last pixel in the array.
- Assume 1000 x 1000 array (1000 pixels/row)
  - Time to scan 1 row = .125 ns x 1000 = 125 ns (TSMC 0.25um)
  - Time to readout cell = 30 bits x 20 ns/bit = 600 ns
  - Plenty of time to find next hit pixel during readout

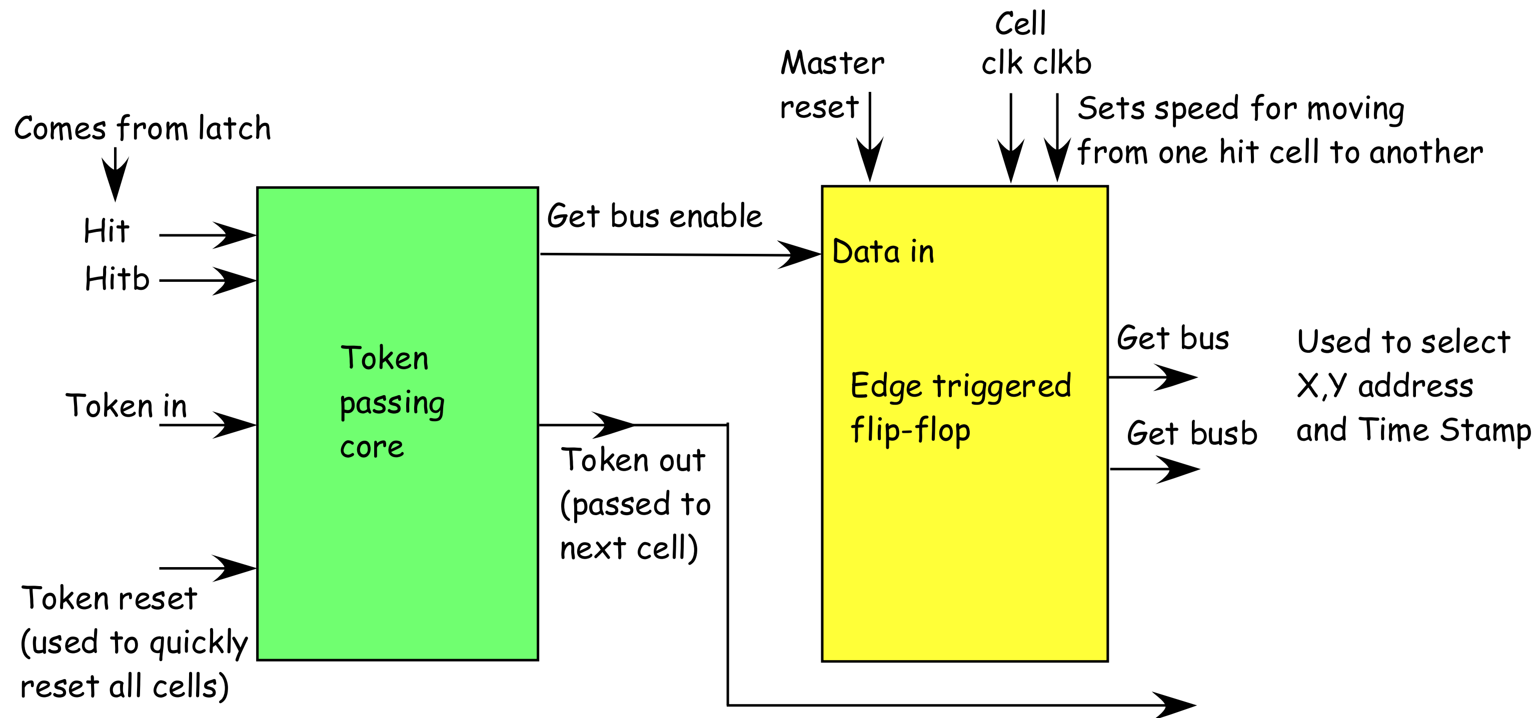
Readout Time

- Chip size = 1000 x 1000 pixels with 15 um pixels.
- Max hits/chip = 250 hits/mm^2 x 225 mm^2 = 56250 hits/chip.
- If you read all pixels with X=1, add 1000 pixels (small increase in readout data).
- For 50 MHz readout clock and 30 bits/hit, readout time = 57250 hits x 30 bits/hit x 20 ns/bit = 34 msec.
- Readout time is far less than the ILC allowed 200 msec. Thus the readout clock can be even slower or several chips can be put on the same bus.
- If CMOS is used, the output power is only dependent on the number of bits and not the length of time needed to readout.

Pixel Cell Block Diagram



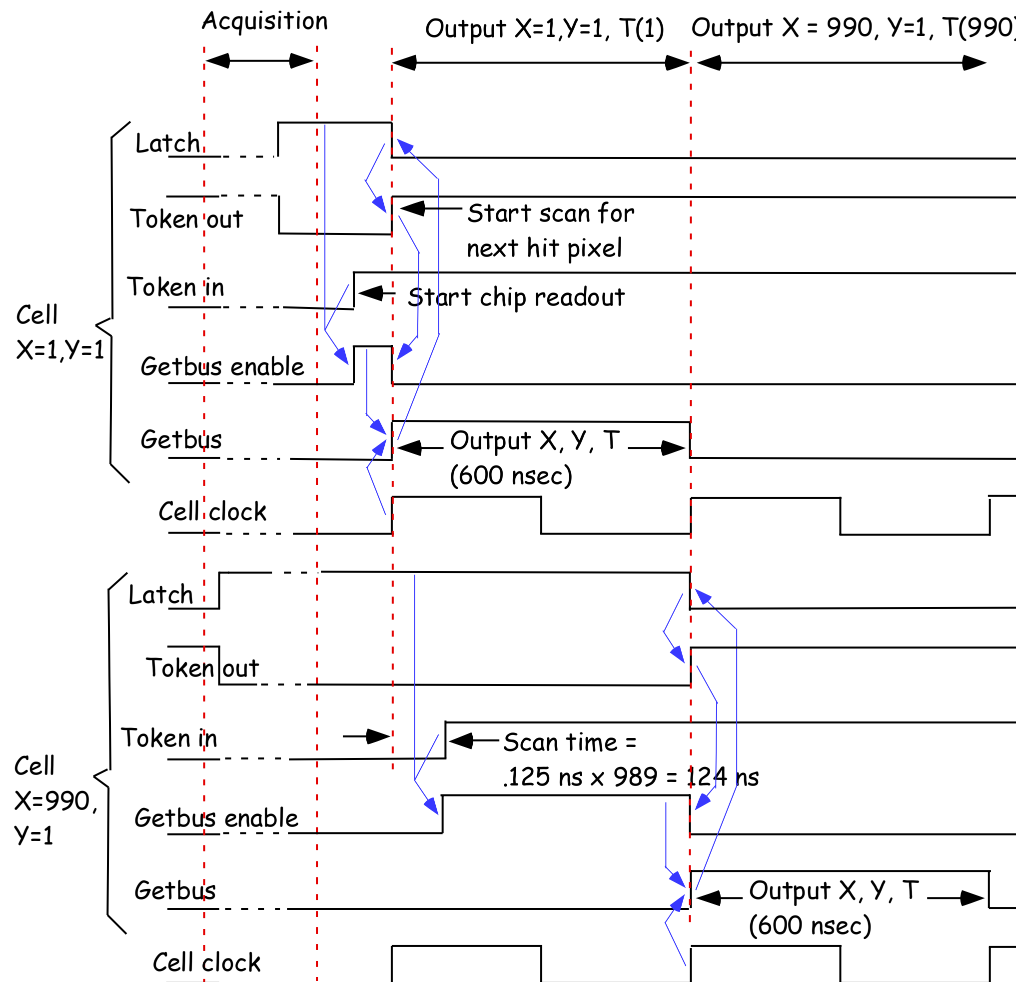
Token Passing Scheme



Core has 13 transistors (can
be reduced to 11
by eliminating token reset
at expense of increasing reset time
but that might not be a problem)

Edge FF has 20 transistors
but could be reduced to 8 if
SR FF is used.

Sparsified Timing Diagram



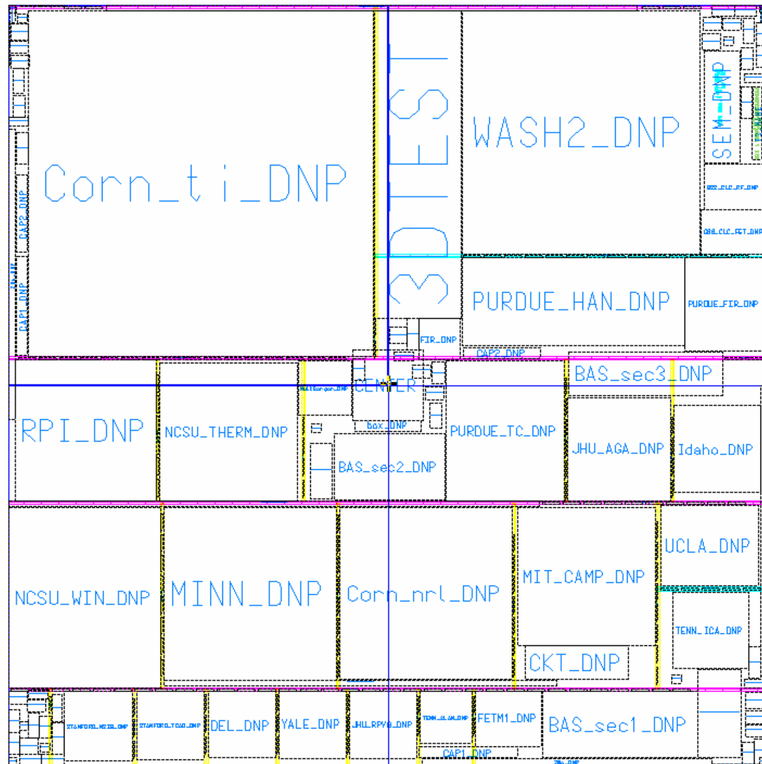
Timing for sparsified readout in first pixel row with hits at x = 1 and x = 990.
Token out from pixel 990 gets passed to pixel x =1, Y = 2 to start readout in second row.

3D Advantages

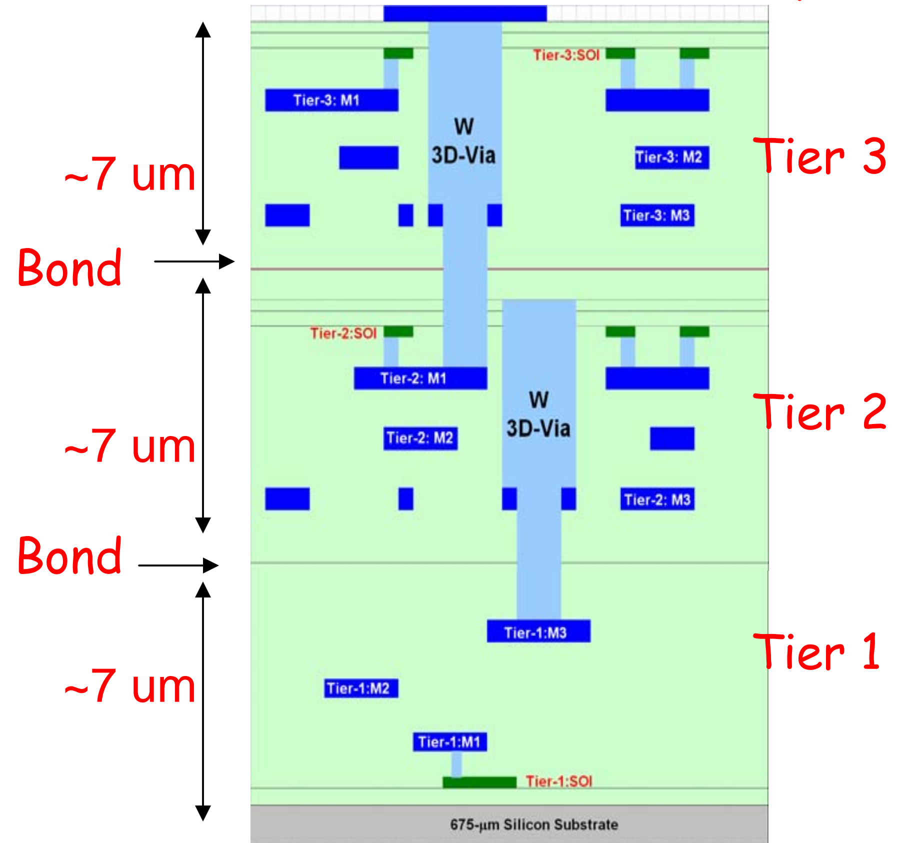
- High resistivity substrate for diodes
- Minimum charge spreading with fully depleted substrate
- 100% diode fill factor
- No limitation on PMOS usage
- SOI for low power
- Increased circuit density without going to smaller feature sizes
- 3D may be used to add layers above other MAPS currently under development.

Chip Fabrication

Fabricate Chip in MIT LL Multiproject run, Oct 1, 2006.
Reticule from previous Multi-project run shown below



Multi-project run has 3 tiers each with 3 metal layers
(3 transistor levels, 11 metal layers)

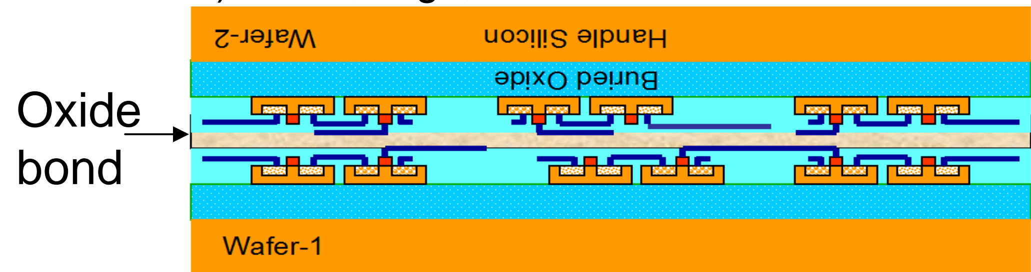


Process flow for 3D Chip

- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

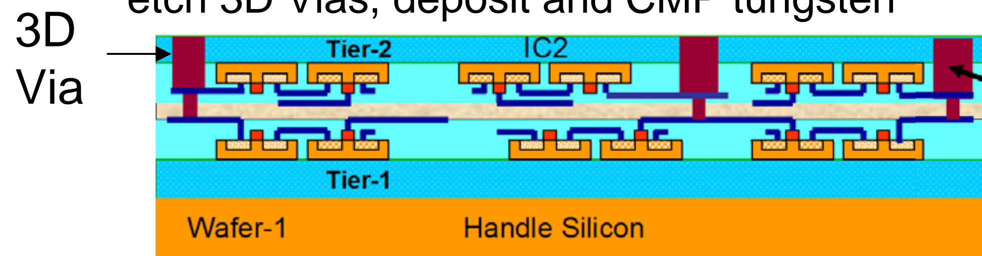
2) Invert, align, and bond wafer 2 to wafer 1

Oxide bond

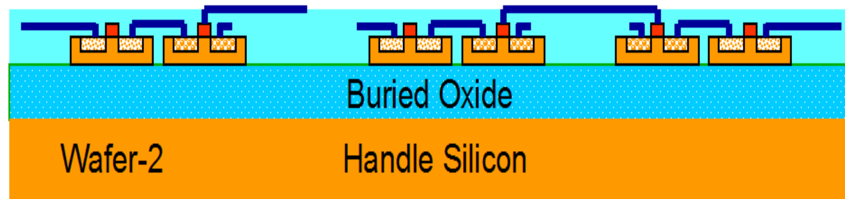


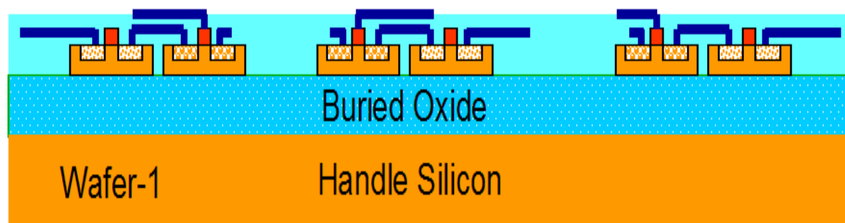
3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten

3D Via

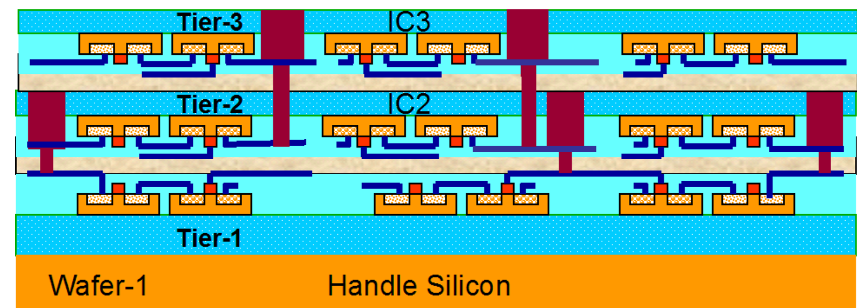


1) Fabricate individual tiers





4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



Conclusion

- Two different 3D electronics efforts are underway at Fermilab
  - Working with existing wafers
    - Thinning
    - Bonding
  - Design of a 3D pixel array with full readout for ILC
- 3D may open new opportunities for HEP
- 3D may be used as an add-on for current MAPS work

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