# Minerva Electronics and the Trip-T

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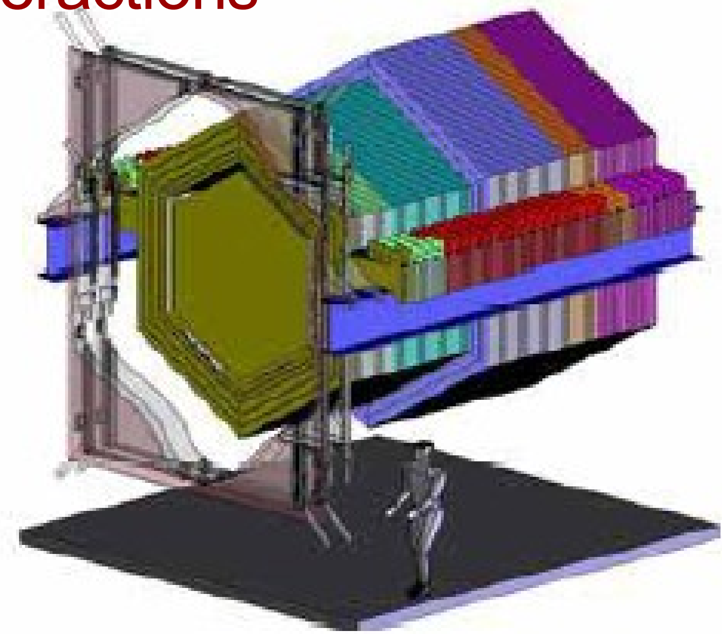
# Minerva Electronics and the TriP-t

- **Outline**
  - Minerva
  - TriP-t
  - The concept for Minerva
  - Overview and status

# Minerva

- **MINERvA is a dedicated neutrino cross-section experiment to be operated at Fermilab in the NuMI (Minos) near hall**
  - "neutrino engineering" for NuMI *et al.*
  - Understand details of neutrino interactions in the few GeV range (of interest for osc. expt's)
  - MINERvA proposes to build a low-risk detector with simple, well-understood technology



# Minerva
# Rules of the Game

**"Low risk… well understood"**

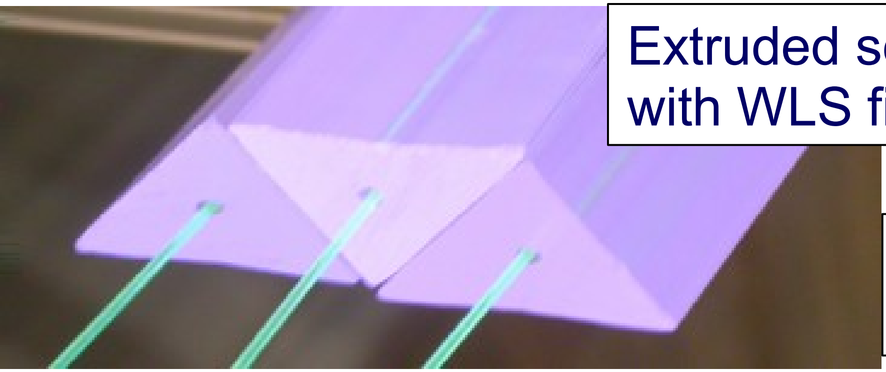
## Use existing technology

Reduces cost, accelerates schedule

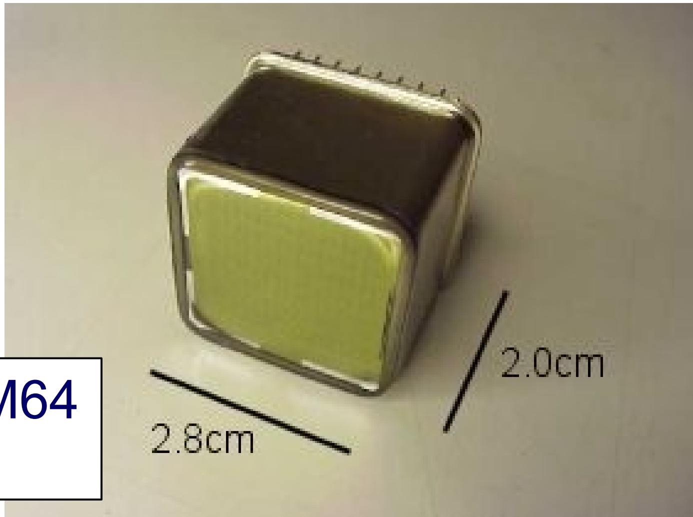
## Active core is extruded scintillator bars

## Surrounded by electromagnetic and then hadronic calorimeters

- Tracking, particle id, energy measurement, few ns timing

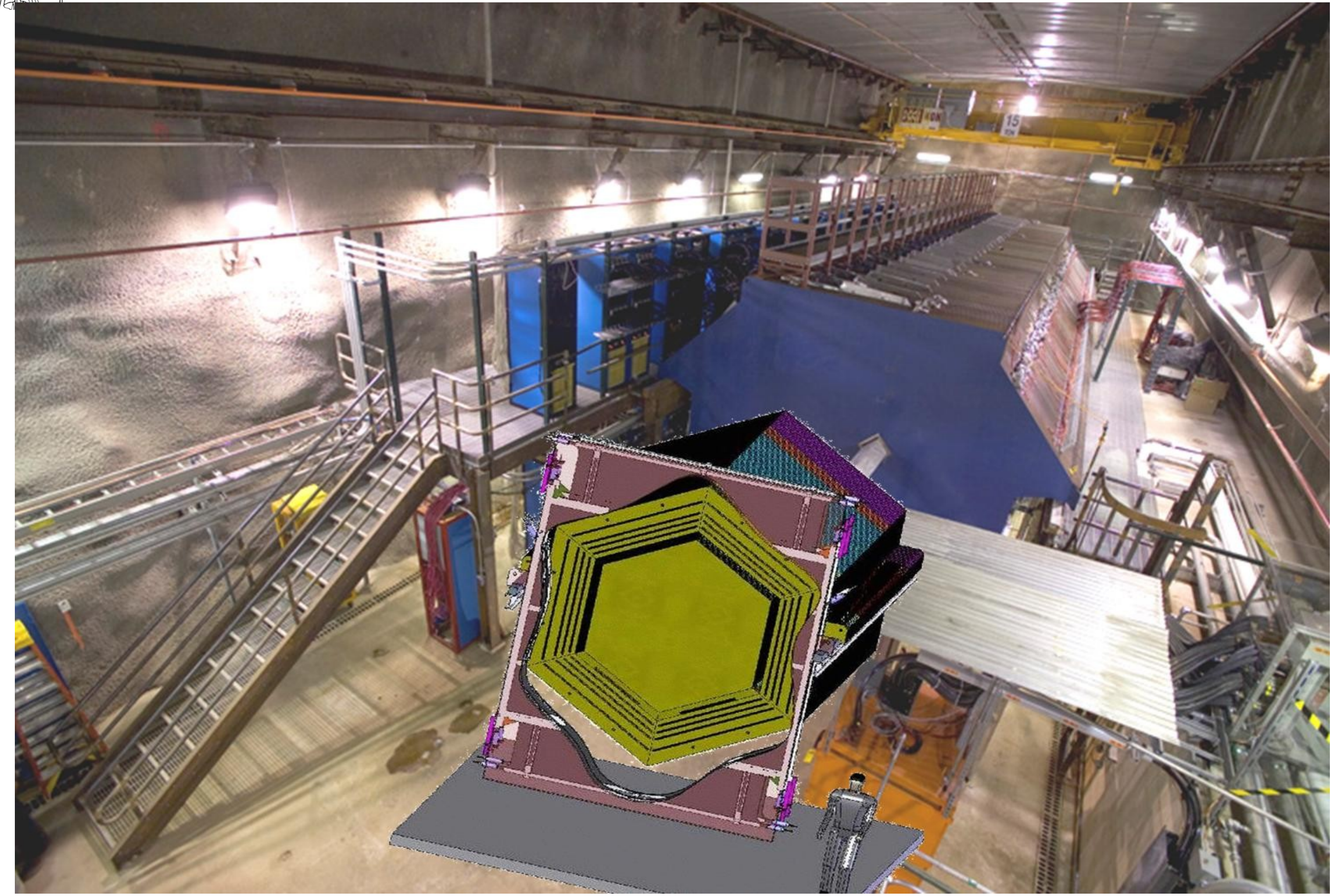


Extruded scint bars with WLS fiber



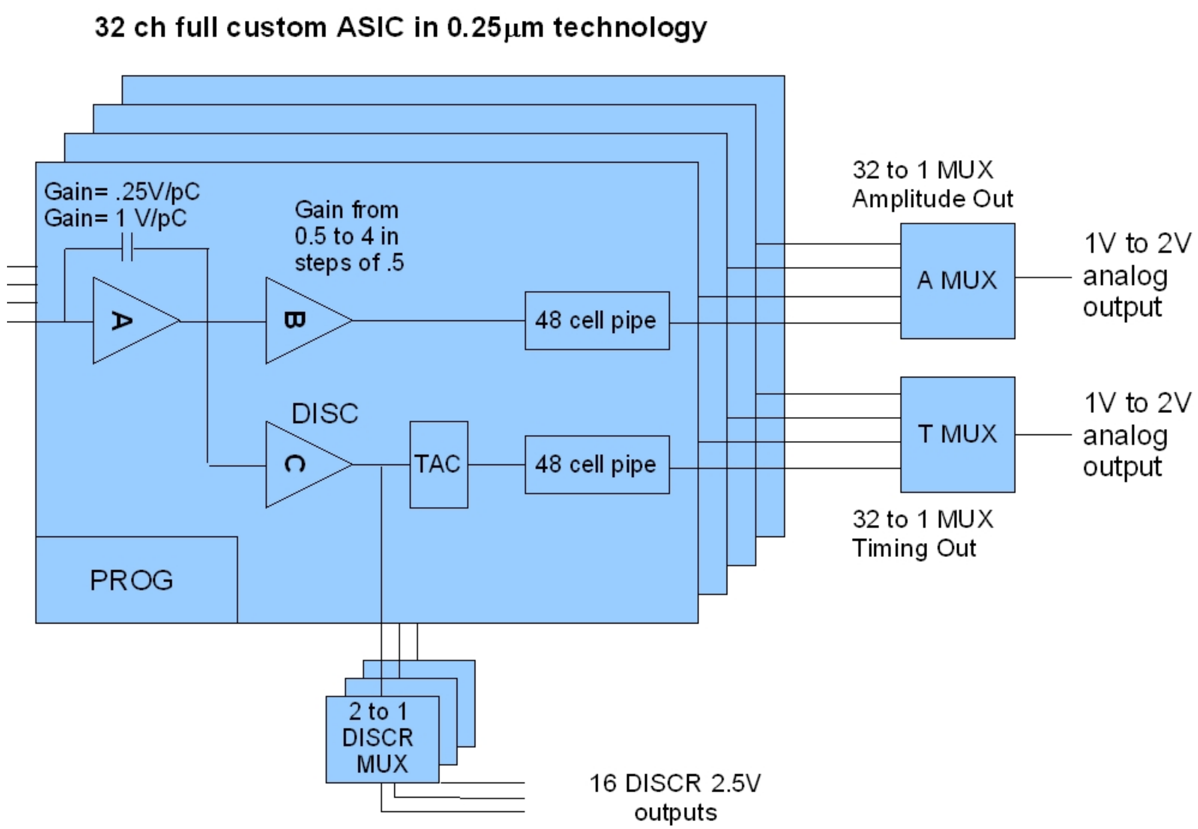

Hamamatsu M64 MAPMT

# Minerva in MINOS near hall

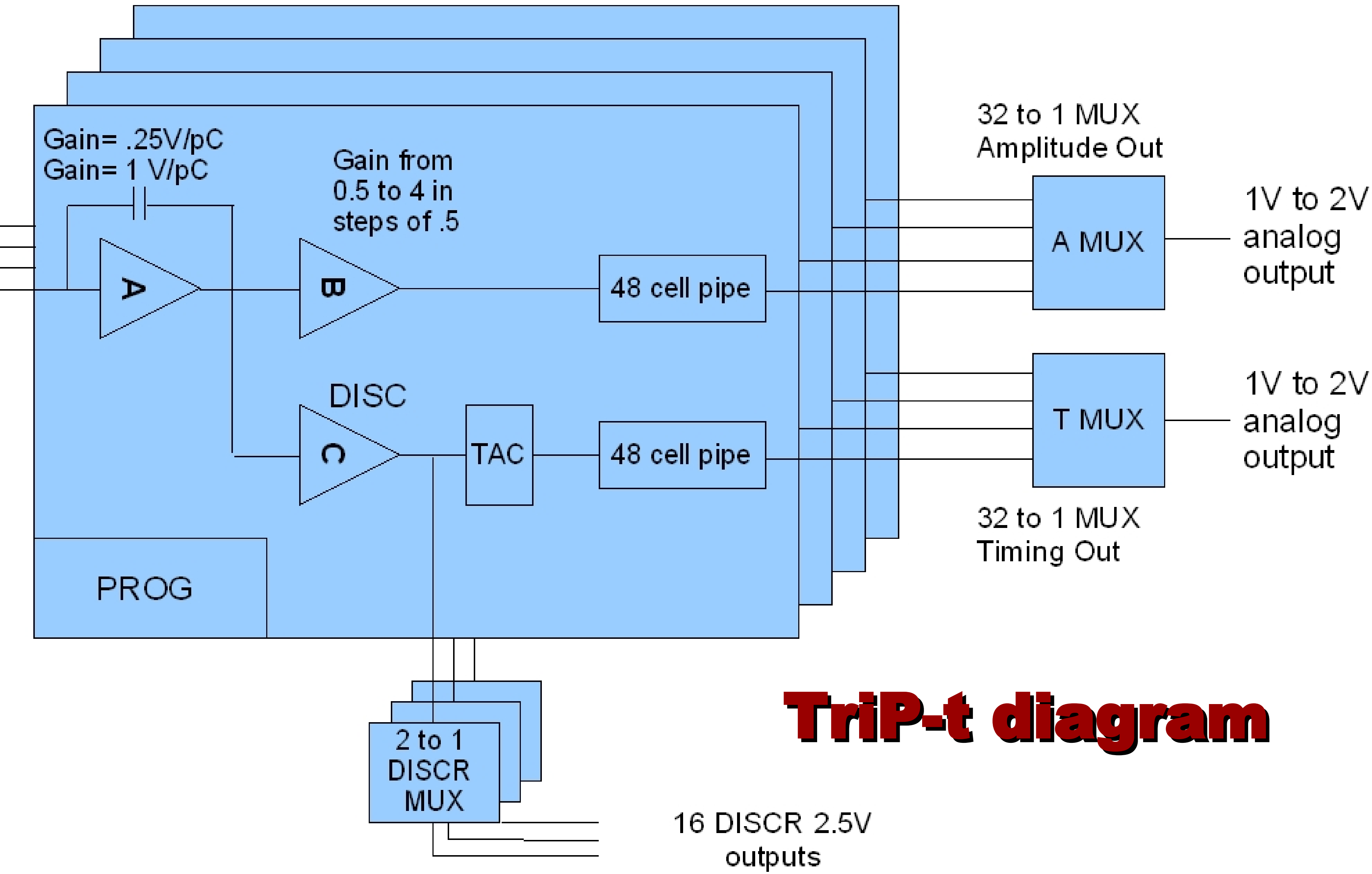


# TriP-t

- **TriP-t: Trigger and Pipeline with timing.**
  - **Full custom ASIC designed at Fermilab**
  - **Not designed for Minerva- designed for Dzero**

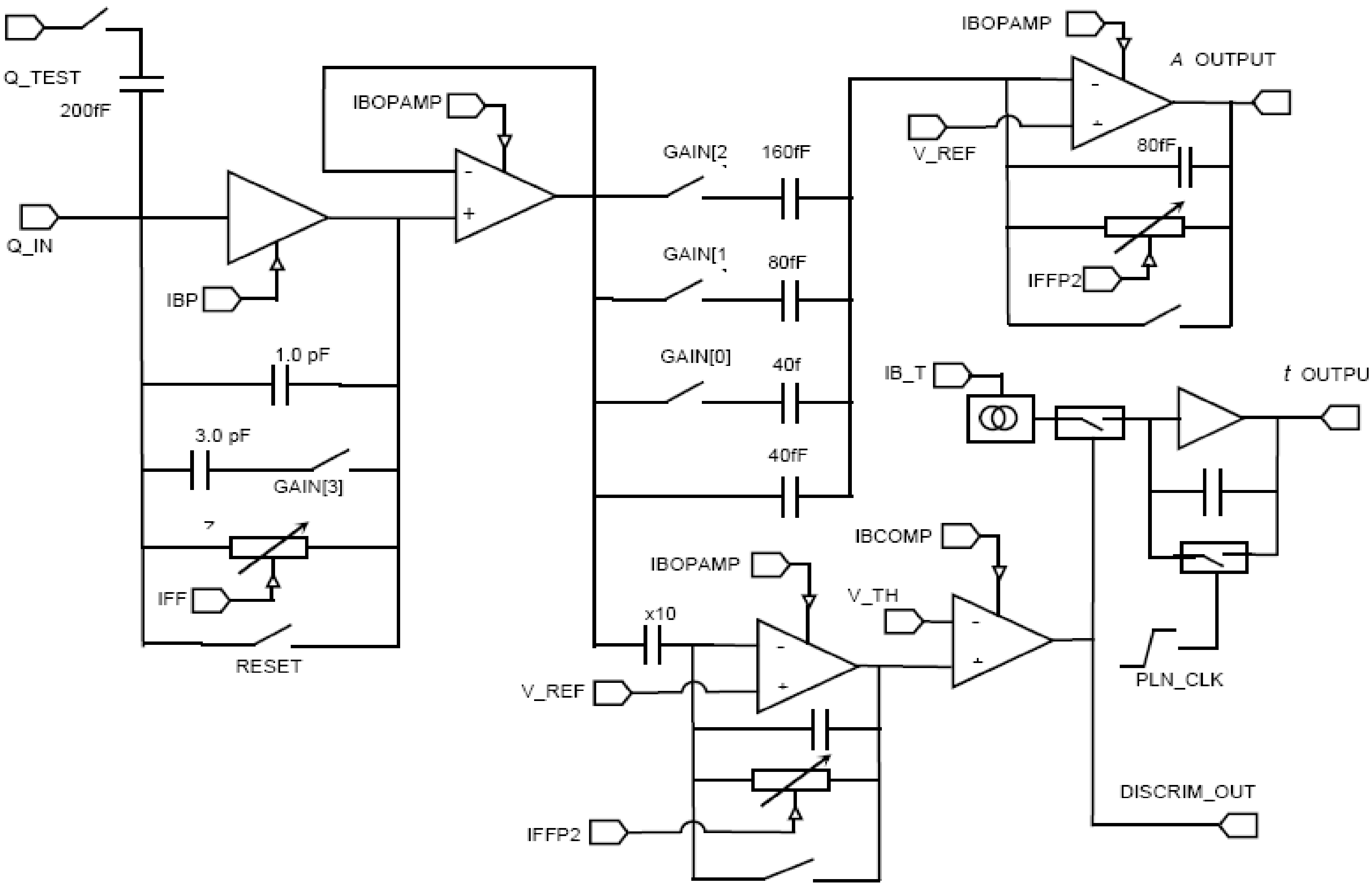


# 32 ch full custom ASIC in 0.25μm technology



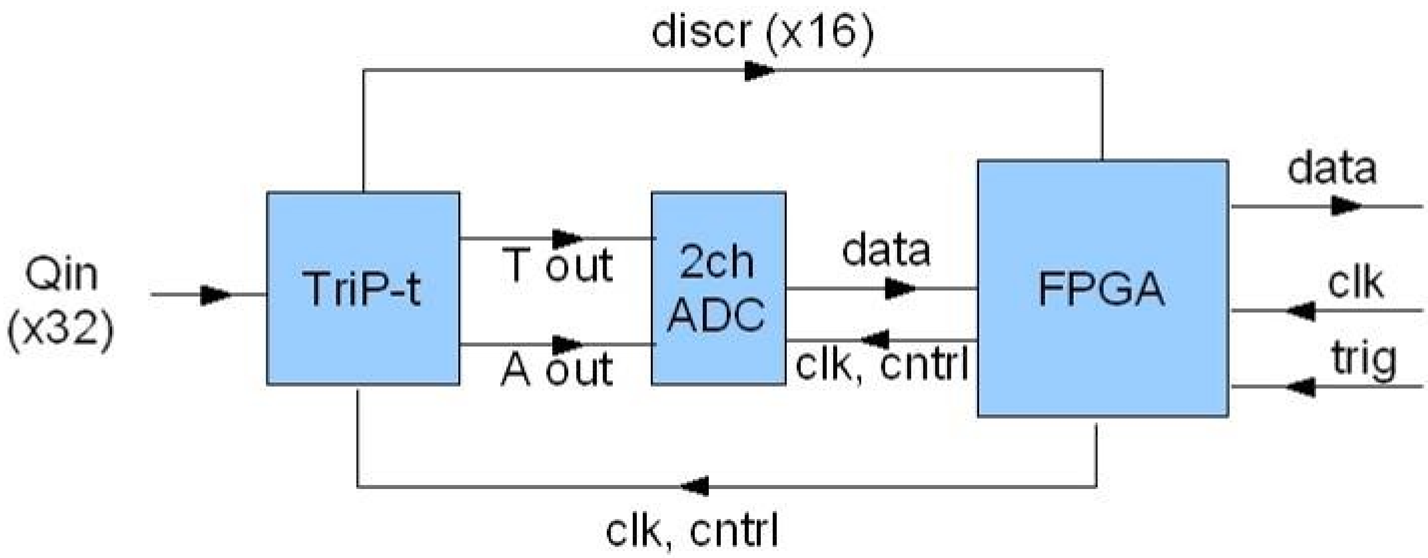

# TriP-t diagram

# TriP-t



Q_TEST
200fF
Q_IN
IBP
IBOPAMP
1.0 pF
3.0 pF
GAIN[3]
IFF
RESET
GAIN[2
160fF
GAIN[1
80fF
GAIN[0]
40f
40fF
IBOPAMP
A OUTPUT
V_REF
80fF
IFFP2
IB_T
t OUTPU
IBCOMP
IBOPAMP
V_TH
x10
V_REF
IFFP2
PLN_CLK
DISCRIM_OUT

# TriP-t typical system




Typical system includes the TriP-t connected to a commercial ADC (10 or 12bit, 3 to 10 MSPS) and an appropriate FPGA.

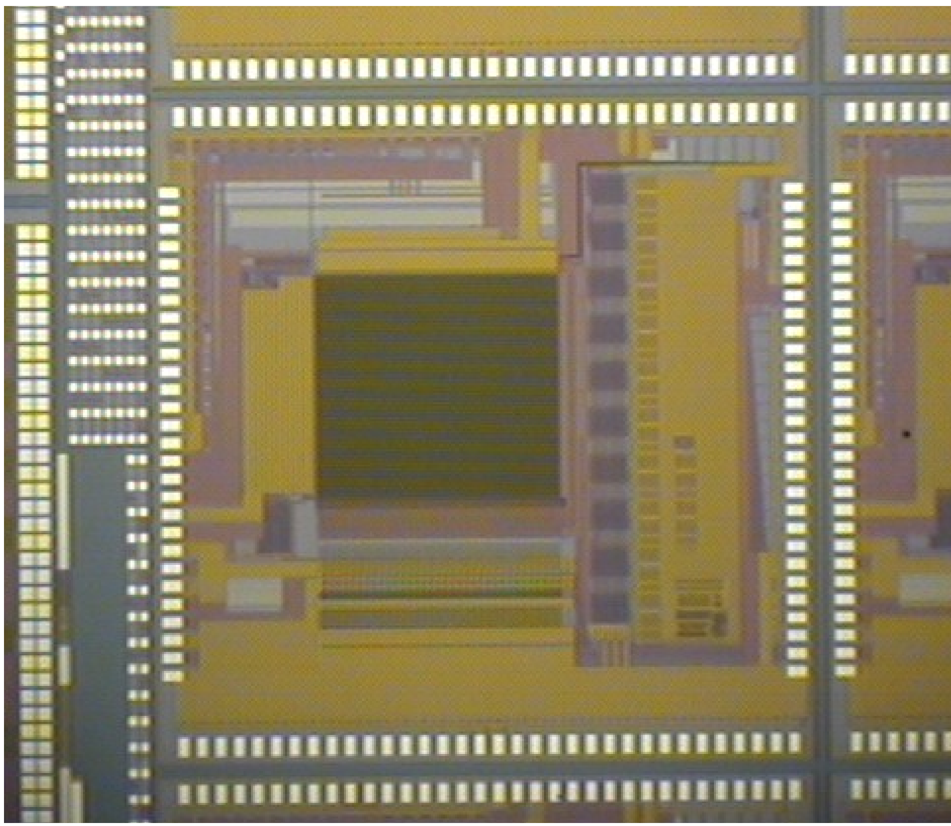
Typically we also use separate LDOs to supply clean 2.5V for TriP-t and ADC $V_{DDA}$

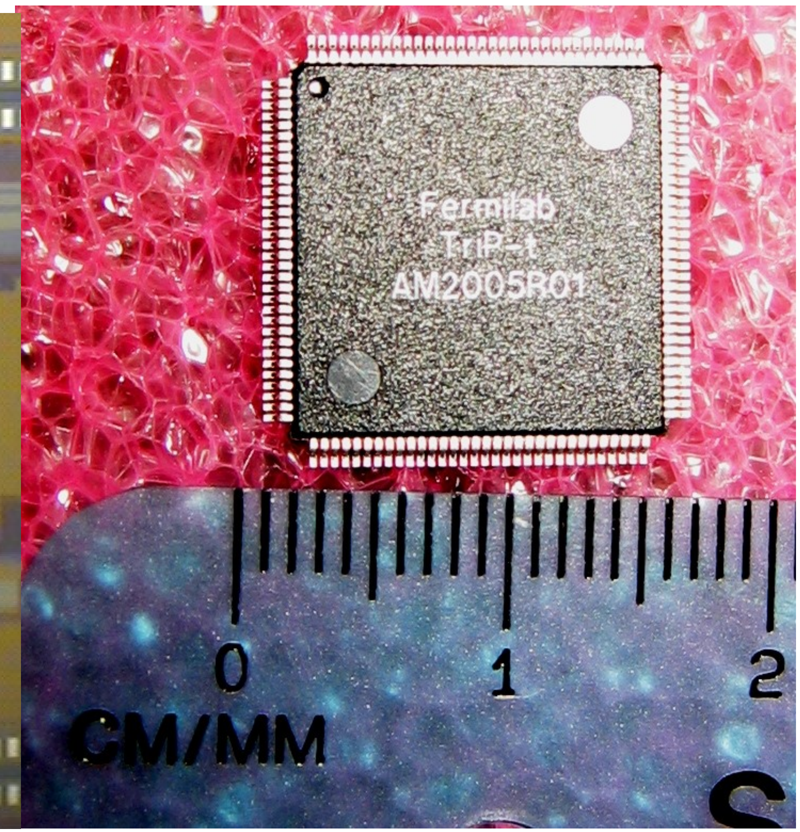
# Key features of the TriP-t

- **Very flexible**
  - Various "clock" signals are brought out
    - preamp reset, 2nd stage amp reset, discr reset, pipeline clock, mux clock and others
  - Many internal bias values are settable via built in DACs
    - Can set shaping time, TAC scale, preamp current, others
    - e.g. for Tevatron, we tested with 132ns bunch spacing
    - For Minerva, we tested with a 12us gate
  - Adjustable gain
    - 1:32 gain range settable with 4 bits
- **Good noise performance (35pF input C)**
    - <1fC RMS, 10fC discr threshold, 1ns timing for Qin>30fC

# TriP-t final product

- Used by Dzero, MICE, MINERvA
- Candidate for T2K





# Minerva and TriP-t

## Minerva needs (30K+ ch)

Noise level 0.2 pe for lowest gain pixels (200K gain)

Large dynamic range ratio of 3-1 in PMT gain >200 pe max signals, so need 11.5 bits

Wish to measure timing with ~2ns accuracy over a 12us spill gate

## TriP-t features

Good noise performance (<1fC at max gain, ~6fC at lowest gain)

Good dynamic range of about 9bits

Will use 2 or even 3ch per input to gain more range

Can use discriminator output to measure timing

Can integrate charge over >10us

# Dynamic range

## We plan to use 2 ch per anode- HG, LG

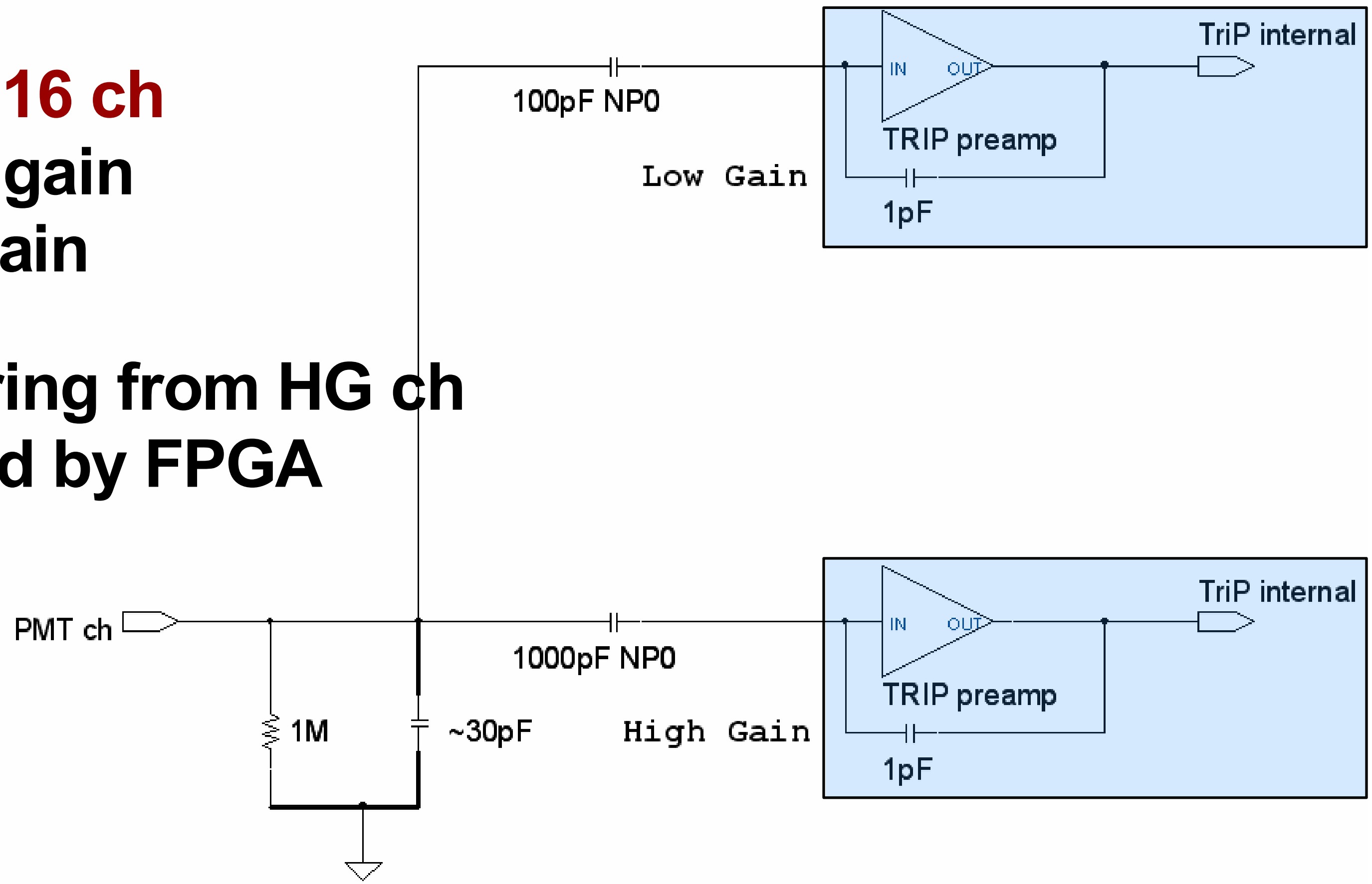
## We can use 3 ch per anode if needed

**TriP-t = 16 ch**

**16 high gain**

**16low gain**

**Discr firing from HG ch recorded by FPGA**



# Gating and timing

- **External "Start Gate" signal (~1Hz) indicates a spill**
- **Wait for a DISCR to fire. If a DISCR fires:**
  - Wait to see if any neighbor is hit!
  - Wait to collect charge from neighbors
  - After a reasonable time, push the pipeline, reset the DISCR, ready to go again
    - Reasonable time = 150 ns
  - Once you do that, might as well reset the integrators.
    - About ~100 ns for all of that
- **Dead time: ~1% per hit**
- **The end of a gate always causes all the charges to be stored**

# Minerva electronics

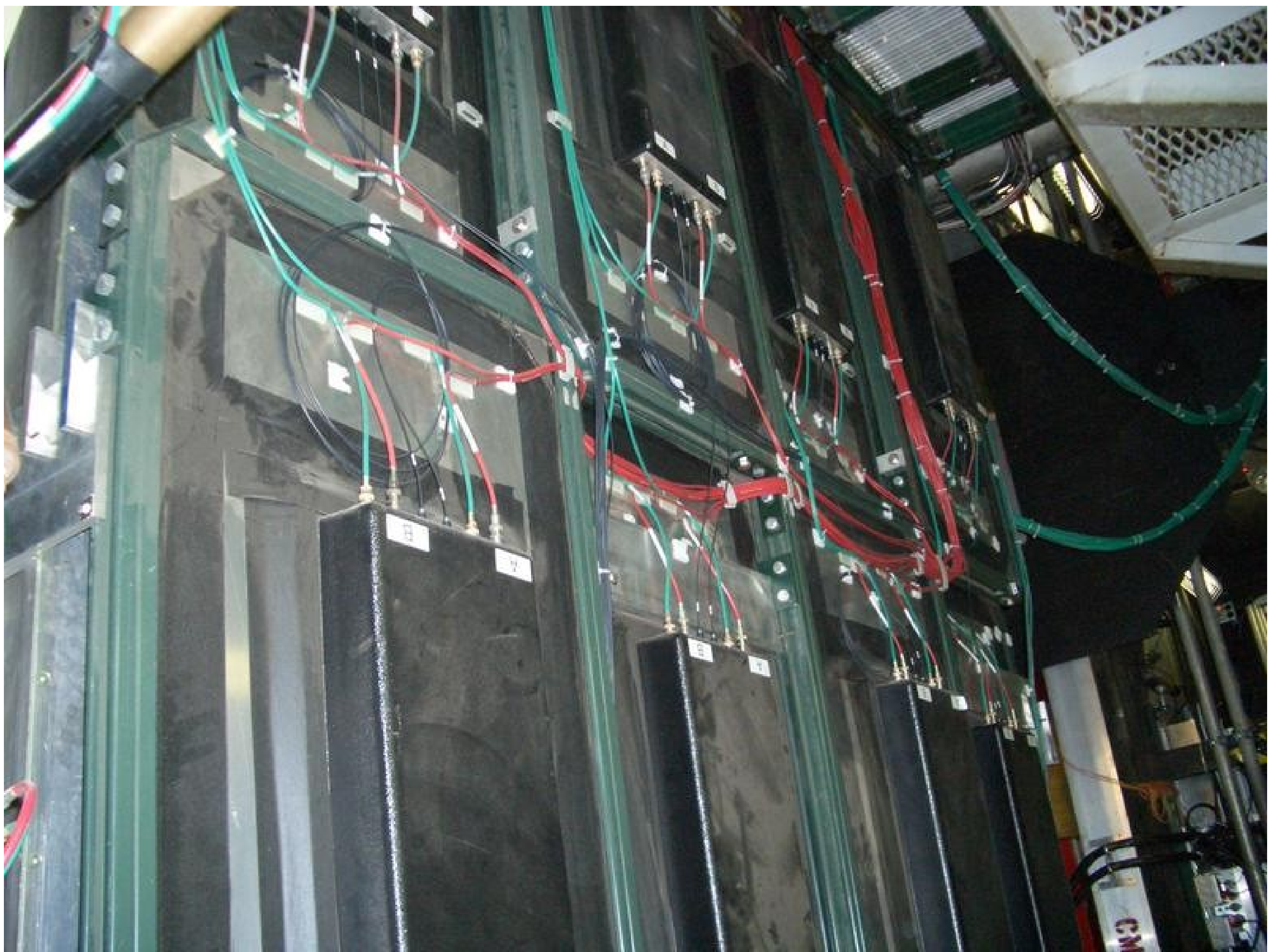
- **Where should PMTs and electronics be placed?**
  - How short can the fibers be?
  - How short can the electrical cables be?
- **We want to measure timing, so we need a good timing mark. How do we get that?**
  - Also wish to correlate events with MINOS
  - MINOS uses a GPS signal and a 53Mhz to tag events. Would like to use the same signals.

# Spaghetti in two flavors

**You can place all the PMTs and electronics in one location - and end up with a mess of fibers (black spaghetti).**

# Spaghetti in two flavors

- **Or you can place the PMTs neatly right at the detector and end up with…**



# Spaghetti in two flavors

## …and end up with the more traditional green spaghetti

# Side Bar

- **It should be understood that the proceeding slides are not meant as a criticism of *any* project or *any* design decision. The point is only to illustrate the line of argument and the decisions made by the team working on the Minerva electronics.**

# Good timing

- Distributing a good timing marker requires a high bandwidth communications channel !

**Captain, we will hit that planet in precisely**

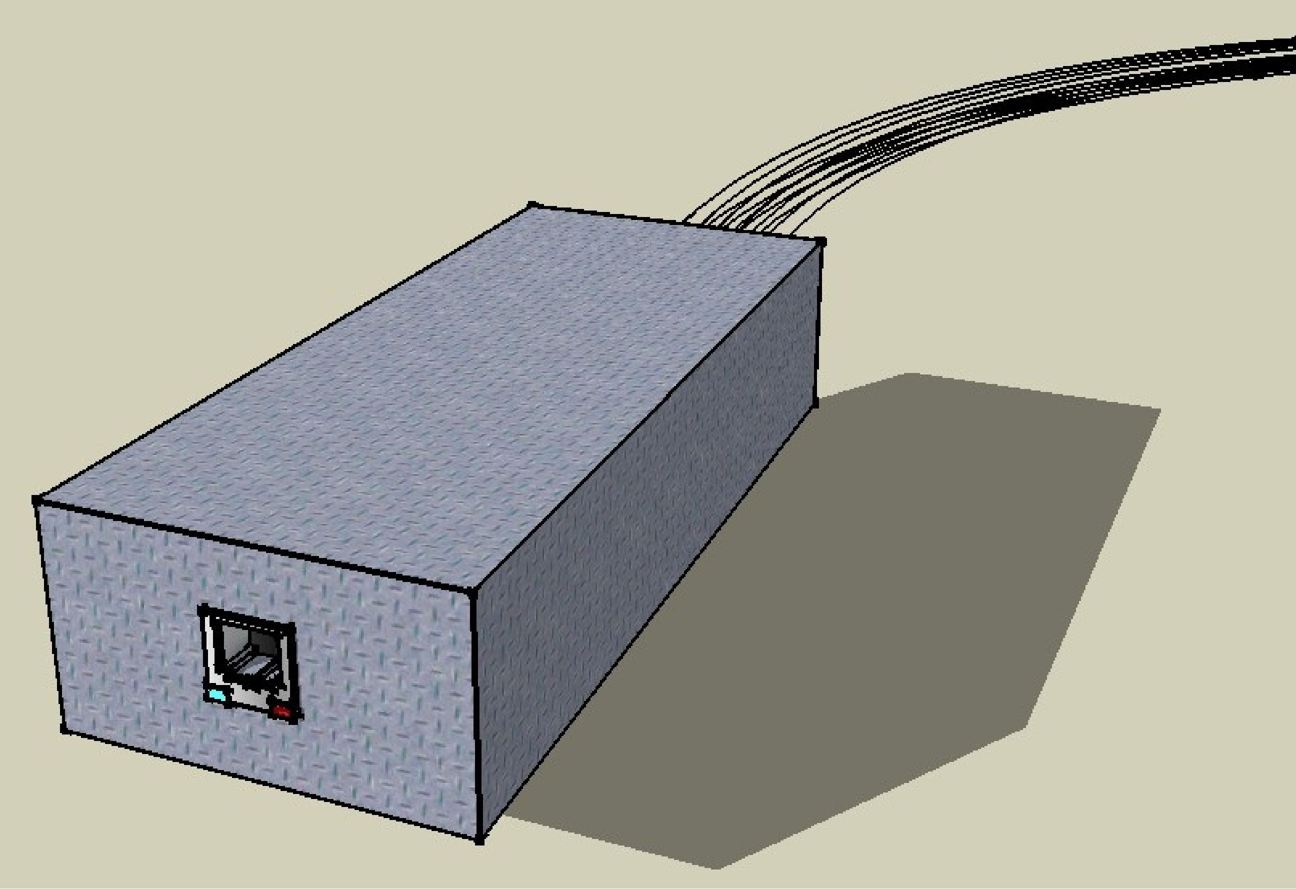
**3.1415926535…**


- Once you have a high bandwidth channel, you can use it to carry not only timing, but all the data, using existing high speed serial standards.

# PMT box dream solution

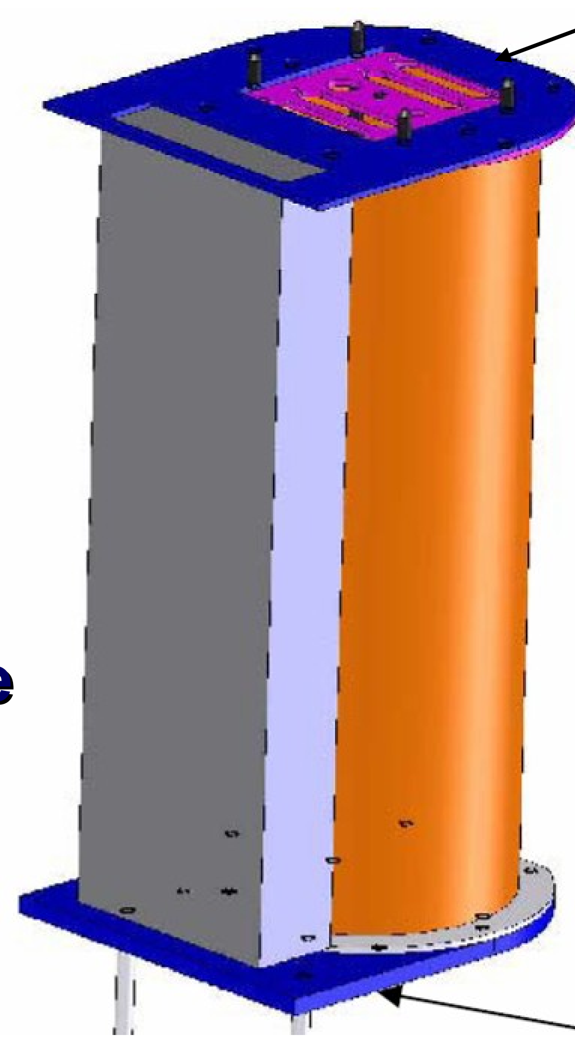
- **Optical fibers go in**

- **Digital data comes out**
  (over something simple, like ethernet)

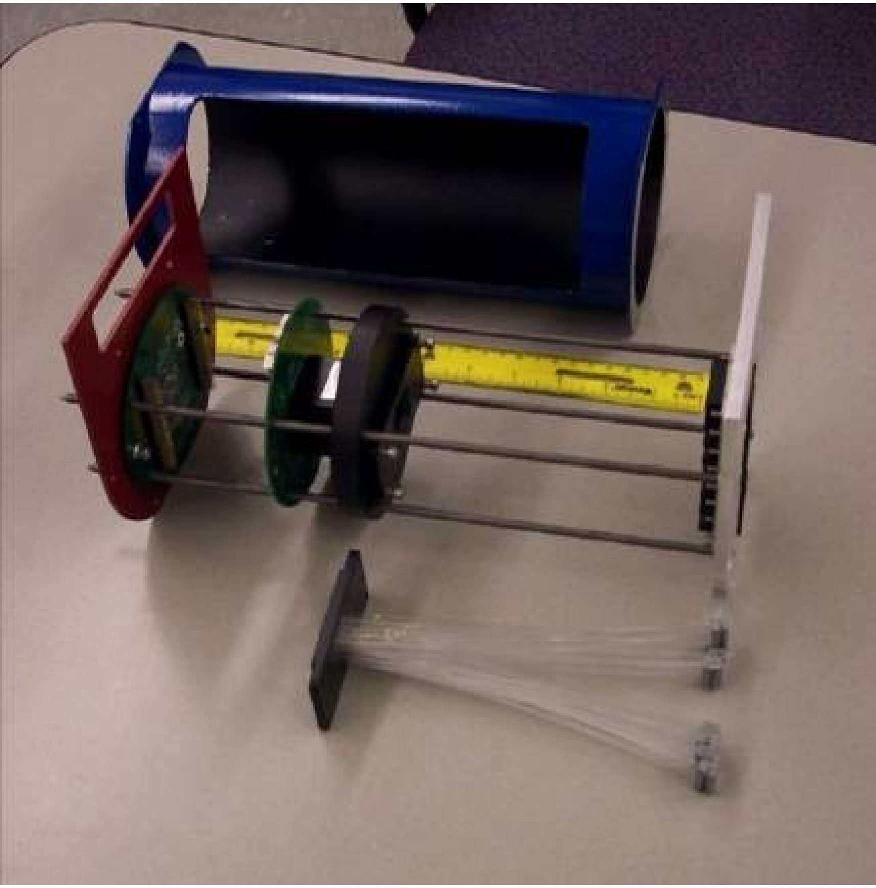


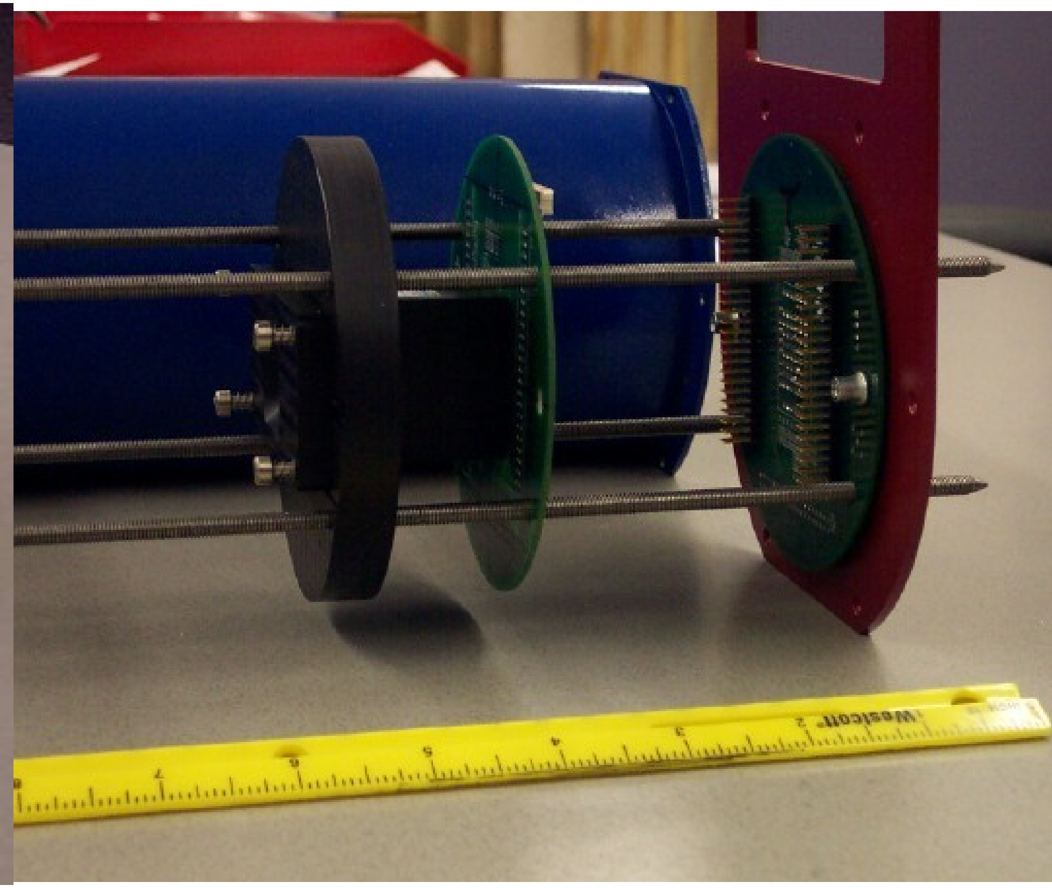
# PMT box reality

**To accommodate production requirements, all active electronics is outside the light tight box. An inexpensive transition board connect the cables running from the base to the Front End board mounted on the top of the PMT box.**

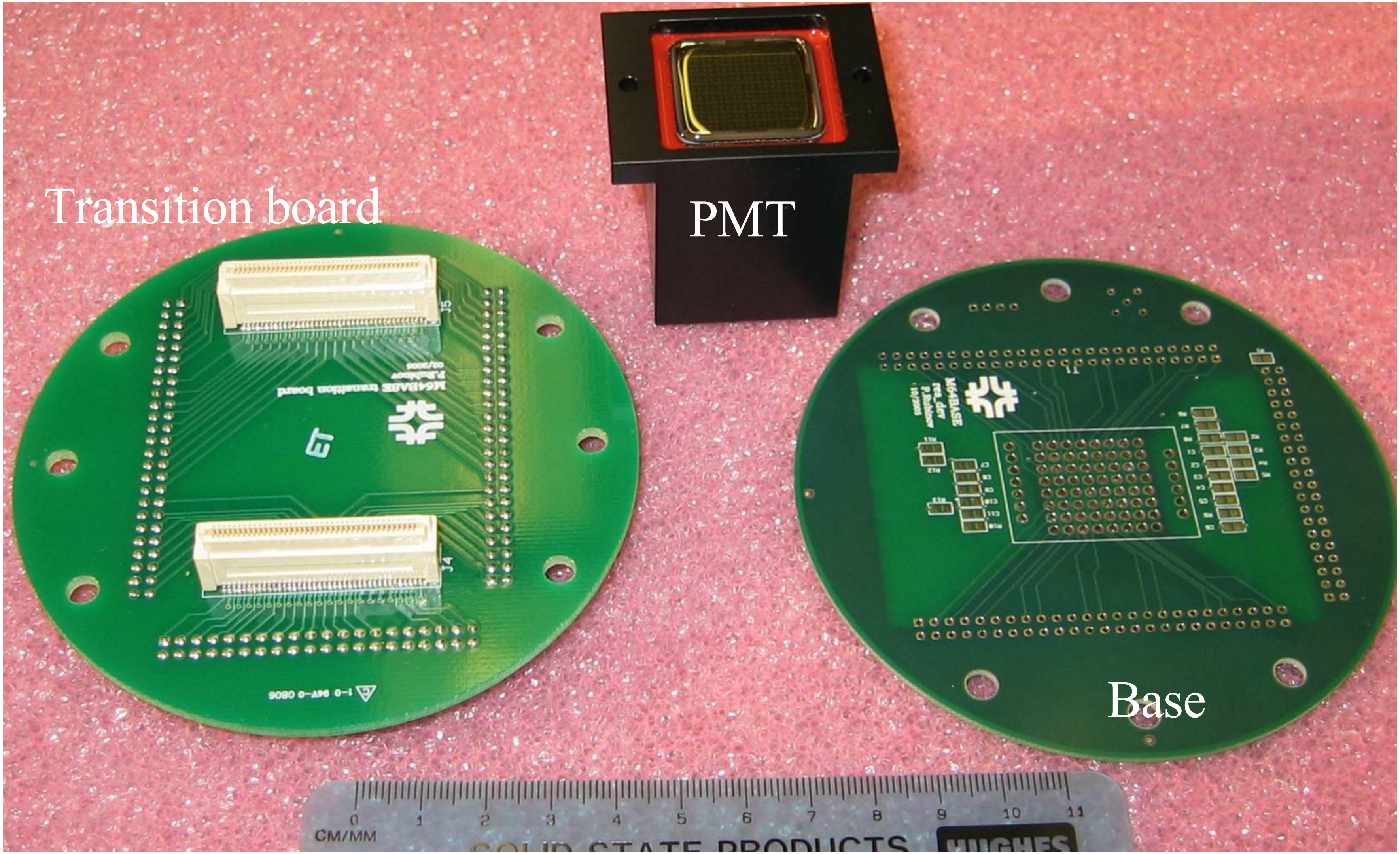


# Inside of the PMT box

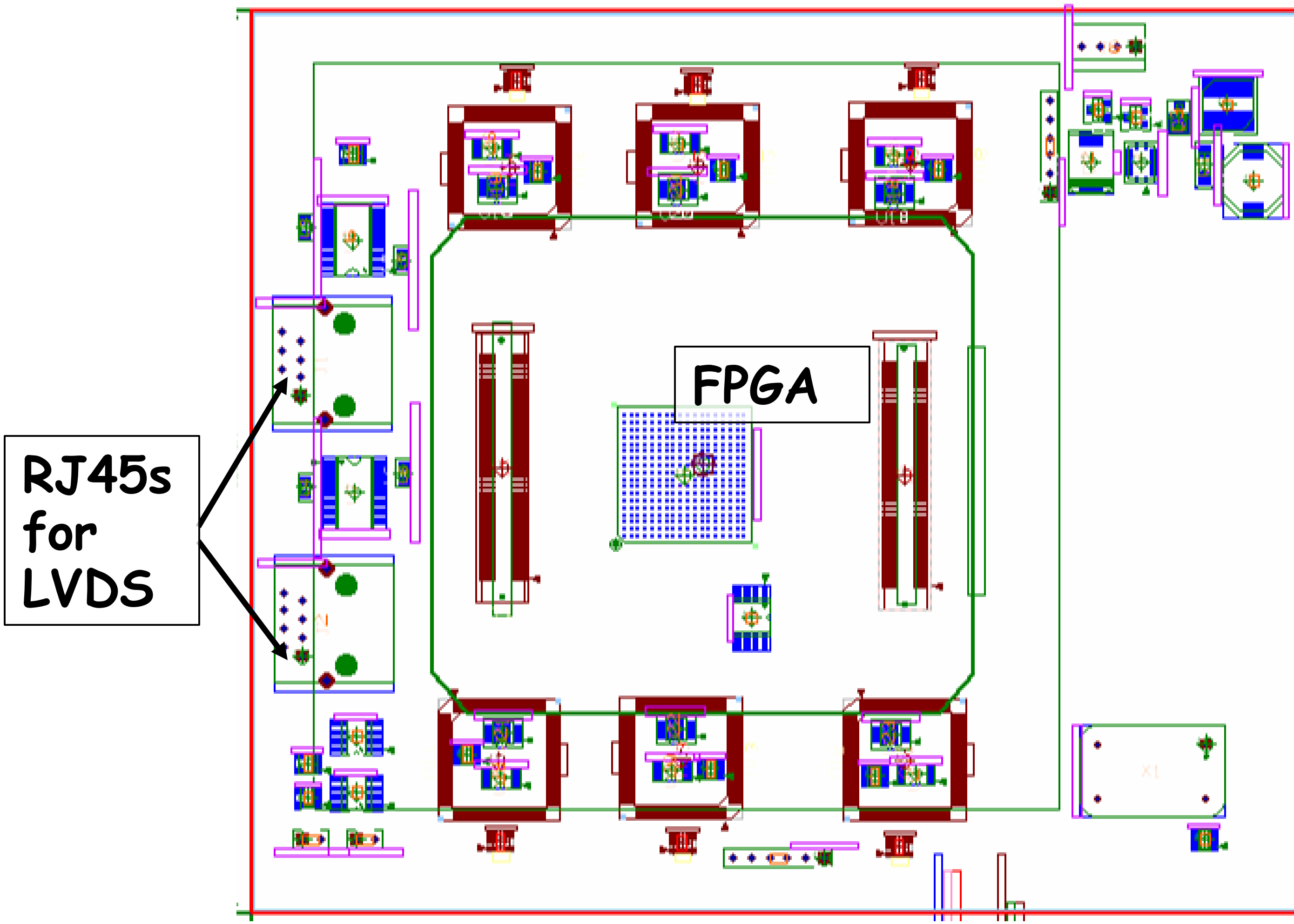




# Spare pictures



# red is bottom, blue is top



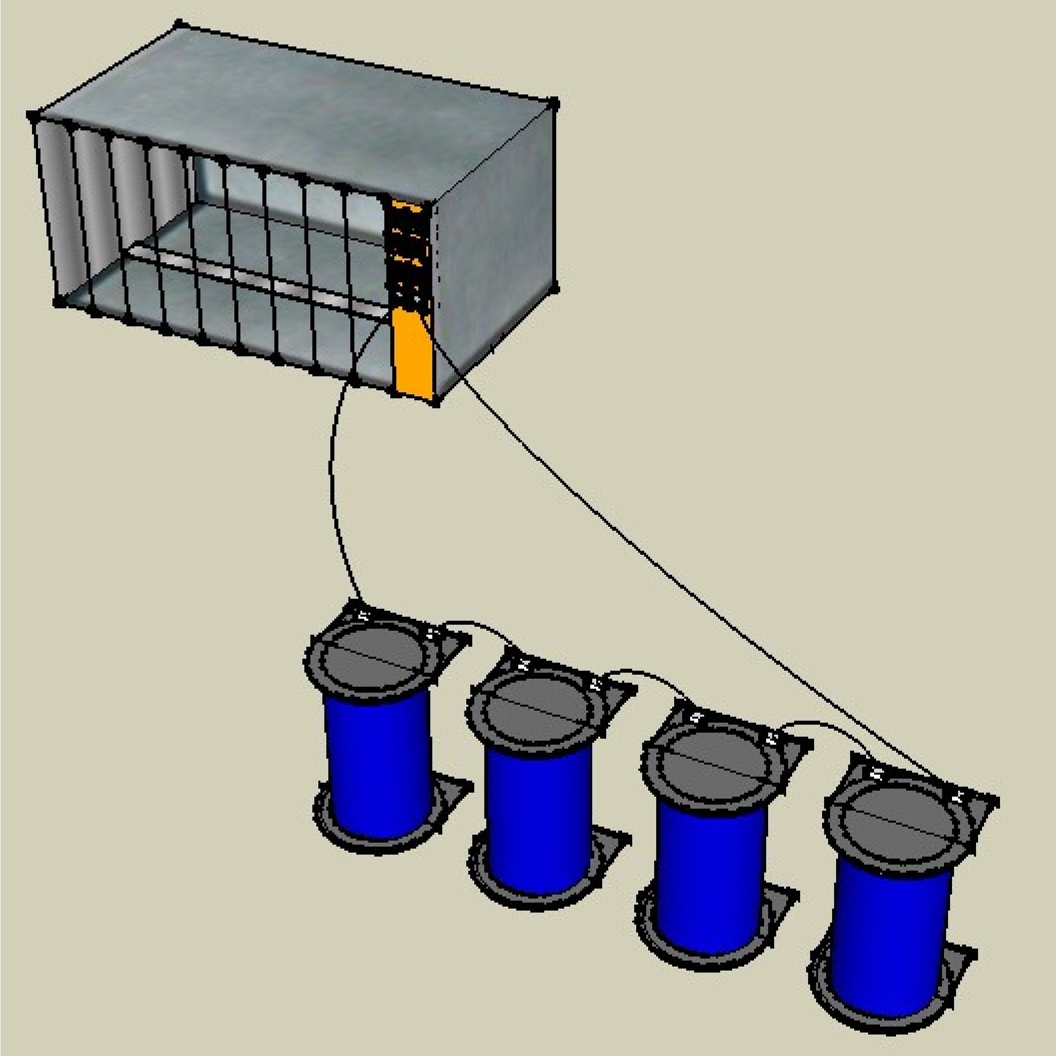
# Readout chain

Each 6U VME readout module supports 4 readout chains.

Each chain has up to 12 FE.

So up to 12 * 4 * 64 = 3072 ch per CROC module.

18 CROC per VME crate -> up to 55K chan per crate.

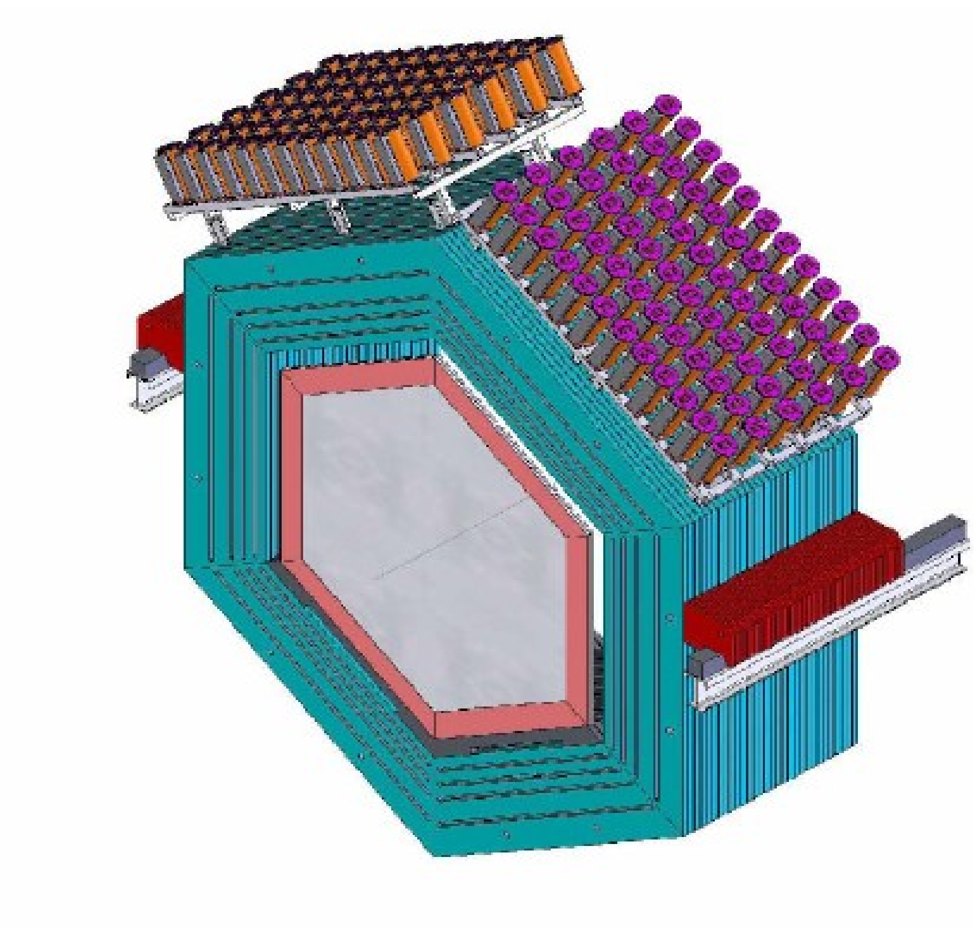


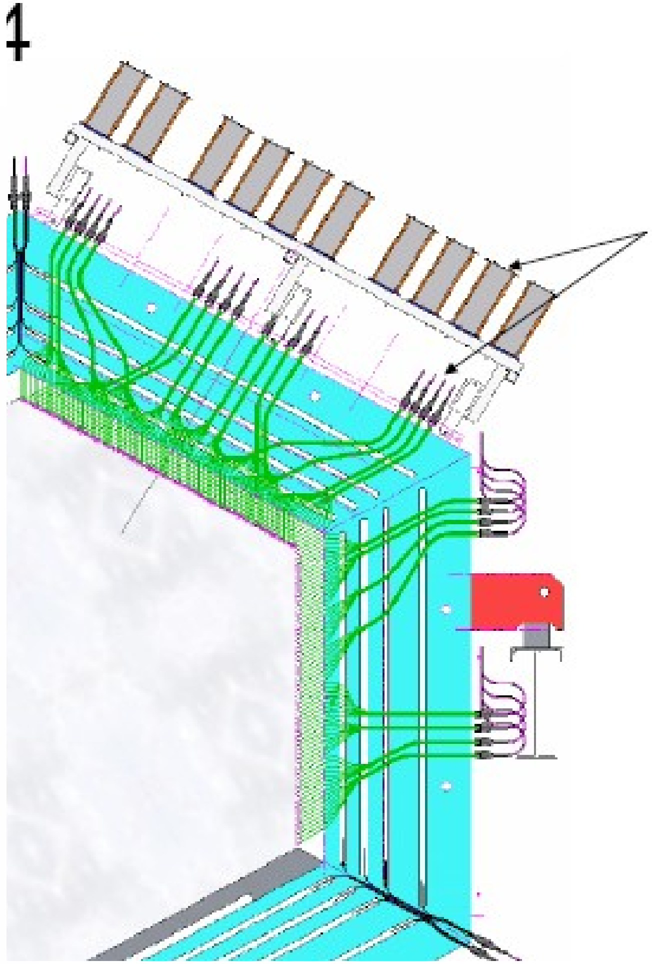
The whole MINERVA experiment will be read out by two 6U VME crates.

# Readout system

- **System is composed of**
  - VME module Chain ReadOut Controller (CROC)
  - Normal CAT5e UTP cables daisy chain PMT Front End (FE) boards
  - Custom protocol but using TI 10bit LVDS chip set running at 13Mhz clk
  - The daisy chain ring carries everything- data, clock, timing markers, configuration commands.
  - 48V power distribution with isolated DC-DC converter on each FE.
  - HV generated by Cockroft-Walton at each PMT box.

# PMT boxes on detector





# Minerva Electronics

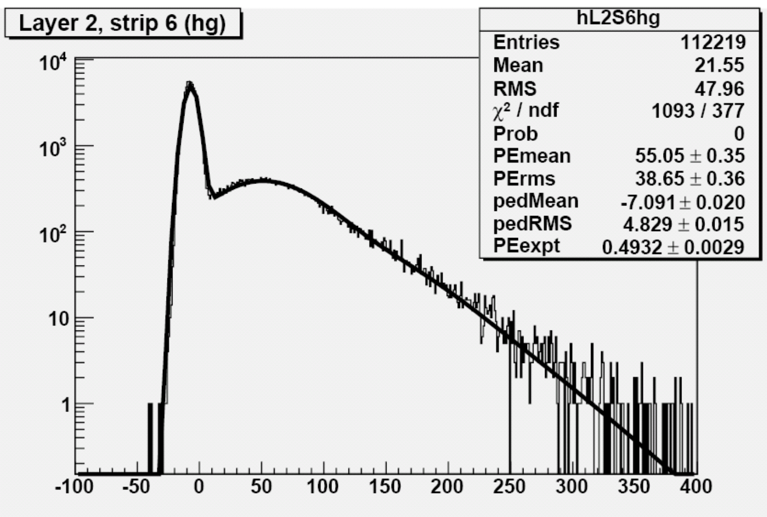
- **Existing technology**
  - TriP-t ASIC designed for Dzero
  - Everything else commercial components
- **Inexpensive, simple**
  - Low data rates, so can use daisy chain scheme with >500 ch per single CAT5e UTP cable
  - Very integrated, self triggering, multi hit front end up to 8 hits per 12us spill, up to 3 ranges per anode

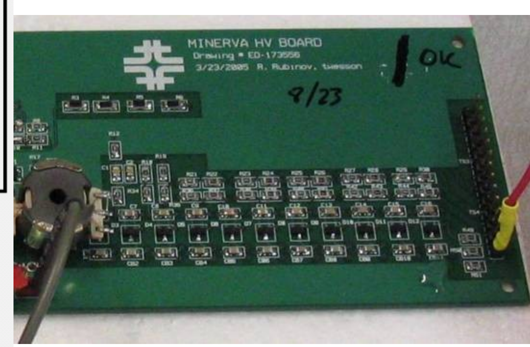
    One power jack (48V, ~10W)

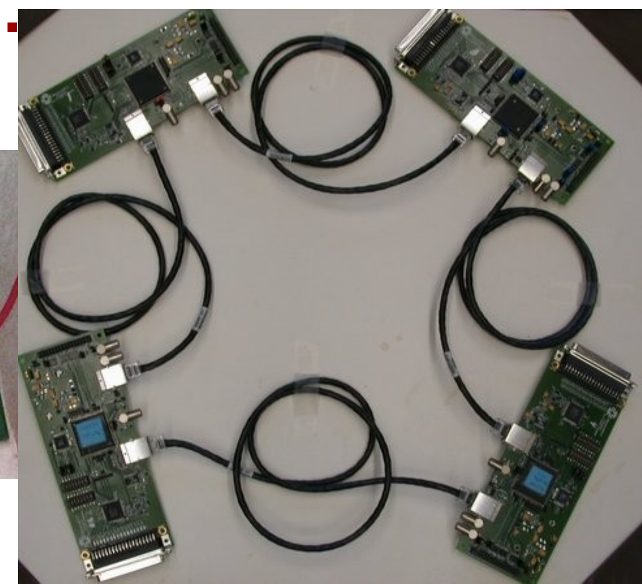
    Two RJ45 jacks (data in and data out)

# Current status

- **Currently working on 2nd round of prototypes**
  - Due by mid summer
- **Basic ideas proven in 1st round of prototypes**
  - LVDS daisy chain can work and has been taken data using the MINOS PMT box.
  - CW design checked out with PMT.



# Credits

## Fermi folks

- Tom Fitzpatrick
- Christian Gingu
- Boris Boldin
- Abder Mekkaoui and the Fermi ASIC group

## Minerva folks

- Kevin McFarland
- Debbie Harris
- Jesse Chvojka
- Vittorio Paolone
- Dave Casper
- Robert Flight

# Spare pictures