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CMOS Monolithic Pixel Sensors for Particle Tracking: a short summary of seven years R&D at Strasbourg

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Outline

- Short history of beginnings
- Review of most important results
- Basic problems, limitations and some solutions
- Near future applications
- Conclusions

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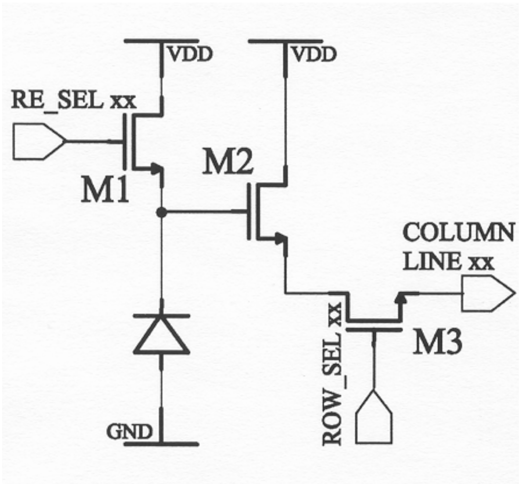
CMOS Active Pixel Sensors for radiation (light) imaging: late 80's (?)

E. R. Fossum, "CMOS image sensors :electronic camera-on-a-chip", IEEE Trans. On Electron Devices 44 (10) (1997)



Basic pixel electronics schemes (photodiode, 3 or 4 transistors, transfer gate…) : all this elements are still bases of today's digital cameras

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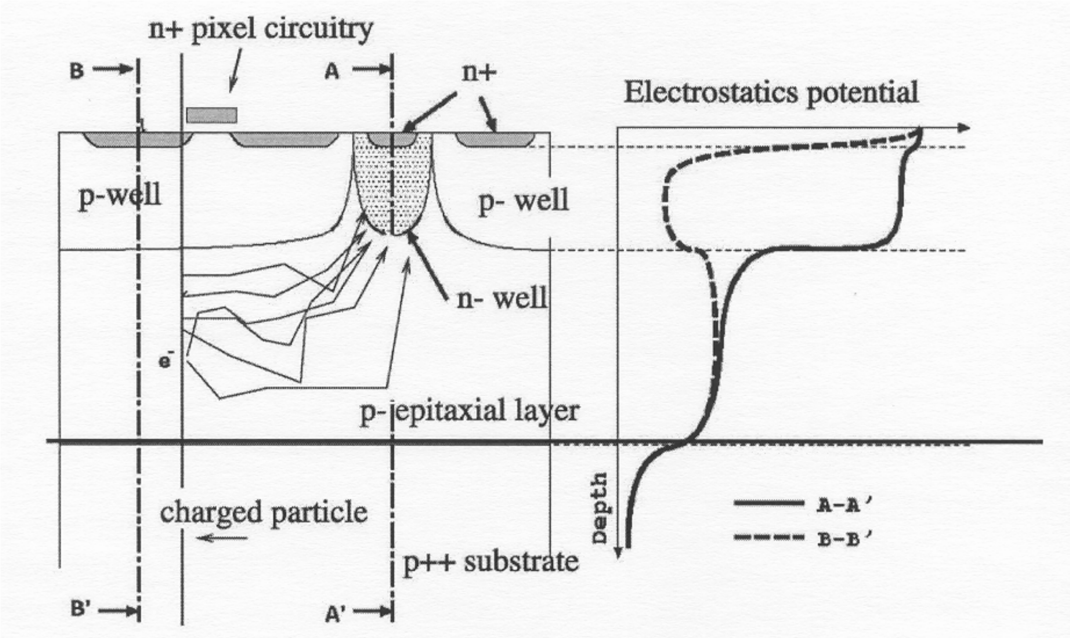
From digital cameras to particle tracking

B. Dierickx, G. Meynants, D. Scheffer "Near 100% fill factor CMOS active pixel sensor", Proc. of the IEEE CCD&AIS Workshop, Brugge, 1997



Twin - tub (double well), CMOS process with epitaxial layer

- **The effective charge collection is achieved through the thermal diffusion mechanism,**
- **The device can be fabricated using a standard, cost-effective and easily available CMOS process,**
- **The charge generated by the impinging particle is collected by the n-well/p-epi diode, created by the floating n-well implantation,**
- **The active volume is underneath the readout electronics allowing a 100% fill factor.**

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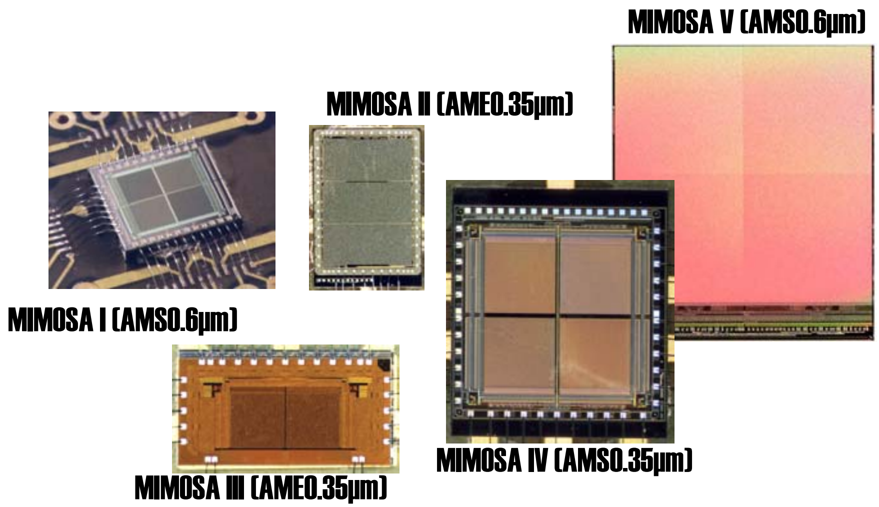
Beginning of MAPS activity at Strasbourg: 1999

Dierickx idea brought to us by R. Turchetta with his own proposition to use it for particle tracking, bought (and financed) by M. Winter from IReS and implemented by LEPSI team (B. Casadei, C. Colledani. W.Dulinski …) backed by a young PhD student from Cracow: G. Deptuch

"Big Bang" → long series of MIMOSA *(Minimum Ionising Particle MOS Active Pixel Sensor)* chips…



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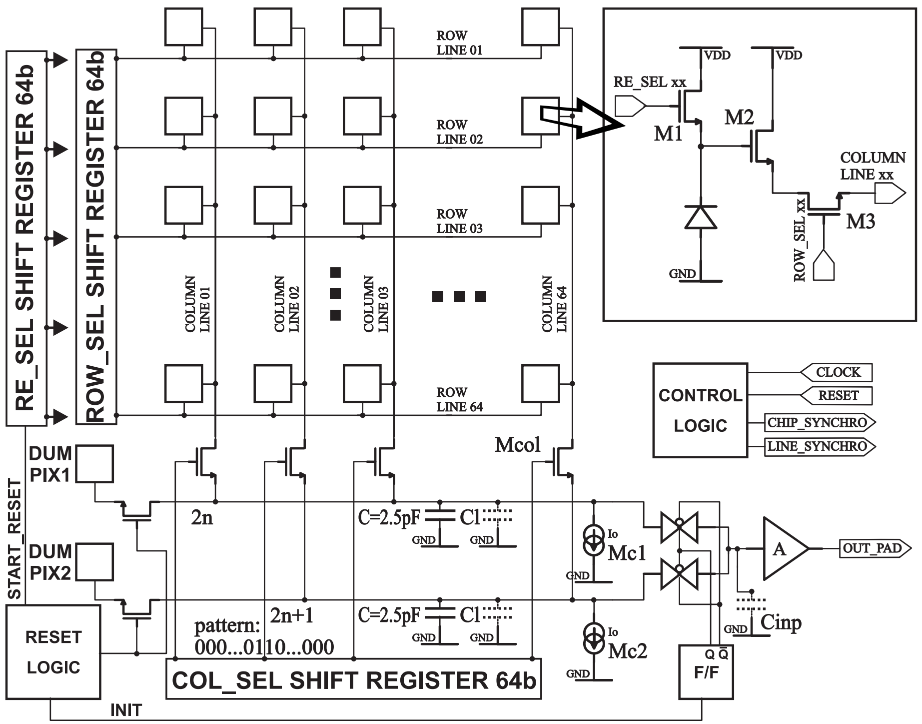
The simplest readout electronics: diode + 3 transistors/pixel

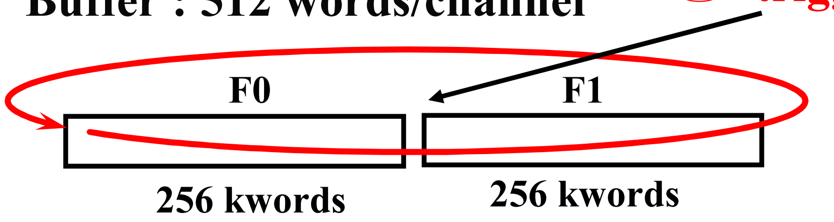


1. Reset in order to inverse bias
2. Continuous serial addressing and readout (digitisation) of all pixels
3. Keeping two successive frames in external circular buffer
4. Following reset when needed (removing integrated dark current)
5. After trigger (or in a real time)), simple data processing in order to recognise hits

Fast ADC 12 bits

Buffer : 512 words/channel

trigger !



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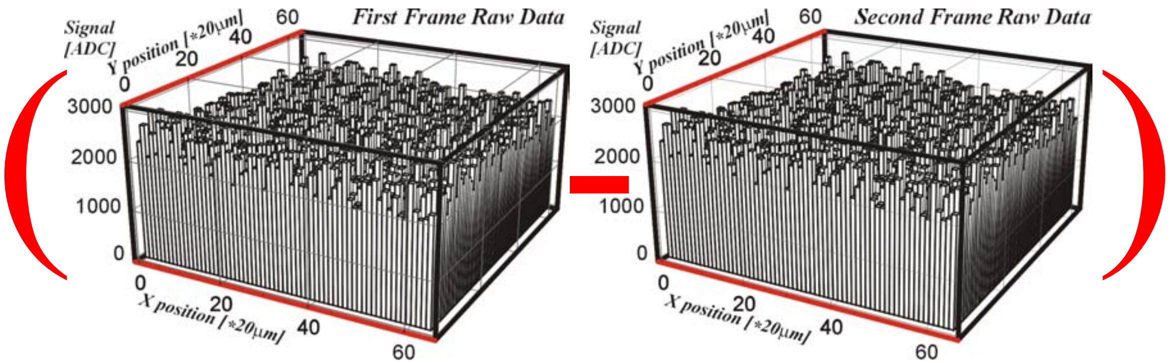
Data processing: (Digital) Correlated Double Sampling



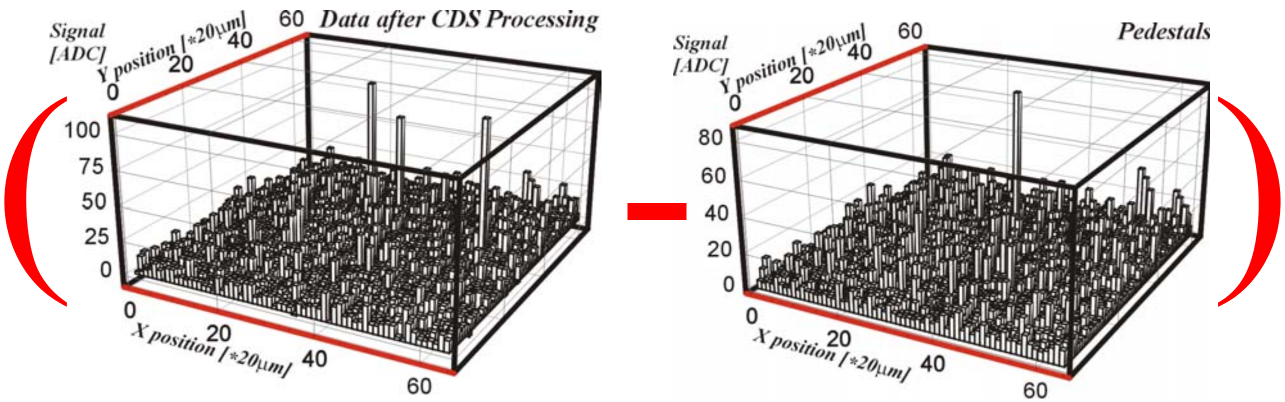
frame 1) frame2)

Useful signal on top of Fixed Pattern DC level

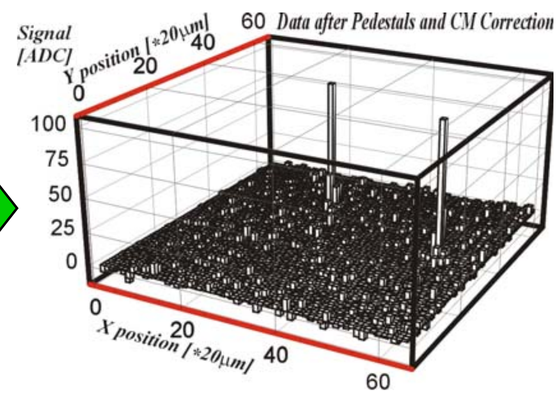
Fixed Pattern dispersion: ~100 mV

Typical signal amplitude: ~1mV

(frame2 - frame1) subtraction



frame2 – frame1) **Pedestal (dark current) subtraction**



Hit candidates!

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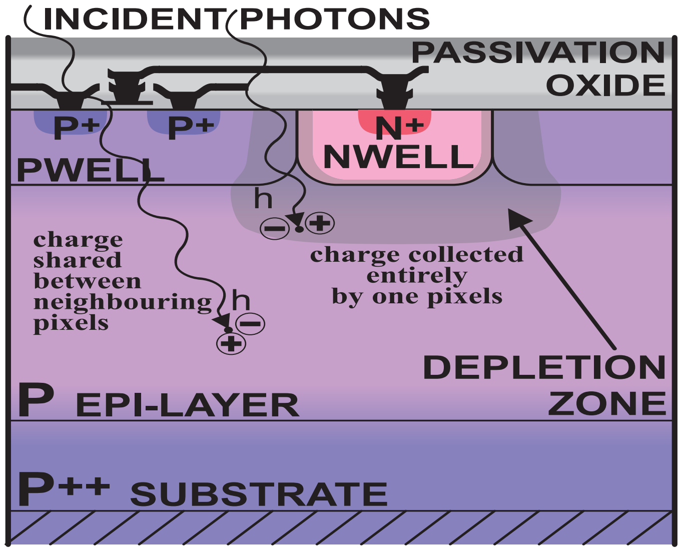
Calibration of the conversion gain - with soft X-rays

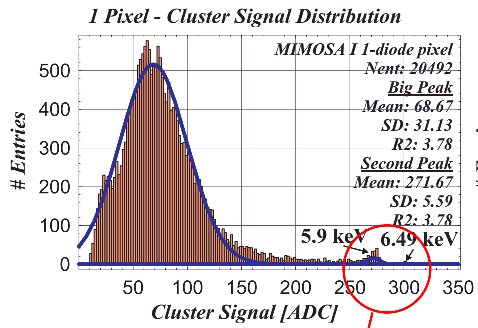
•Calibration methods:

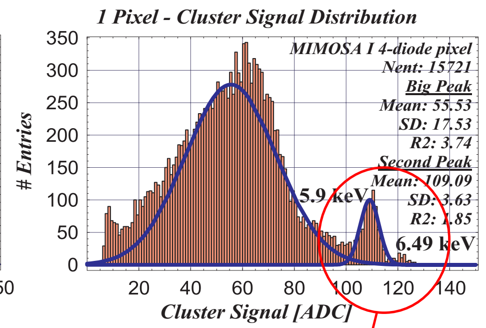
Emission spectra of a low energy X-ray source e.g. iron ^{55}Fe emitting 5.9 keV photons.

very high detection efficiency even for thin detection volumes - μ =140 cm²/g, constant number of charge carriers about 1640 e/h pairs per one 5.9 keV photon



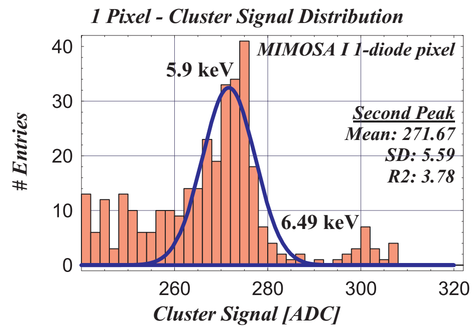
The ' warmest ' colour represents the lowest potential in the device

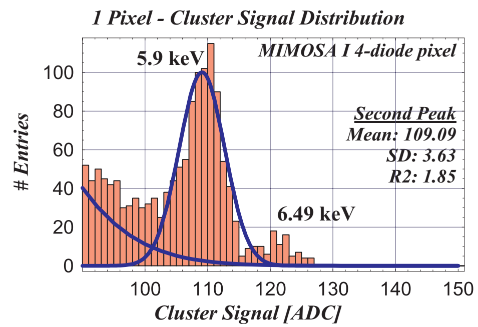




MIMOSA I (14 µm EPI) configuration with single diode in one pixel

MIMOSA I (14 µm EPI) configuration with four diodes in one pixel





MIMOSA I CMOS 0.6 µm	1 diode – 14.6 µV/e⁻	4 diode – 6.0 µV/e⁻
	ENC = 14 e⁻ @1.6 ms f. rate	ENC = 30 e⁻ @1.6 ms f. rate
MIMOSA II CMOS 0.35 µm	1 diode rad. tol.– 22.9 µV/e⁻	2 diode rad. tol.– 17.5 µV/e⁻
	ENC = 12 e⁻ @0.8 ms f. rate	ENC = 14 e⁻ @0.8 ms f. rate

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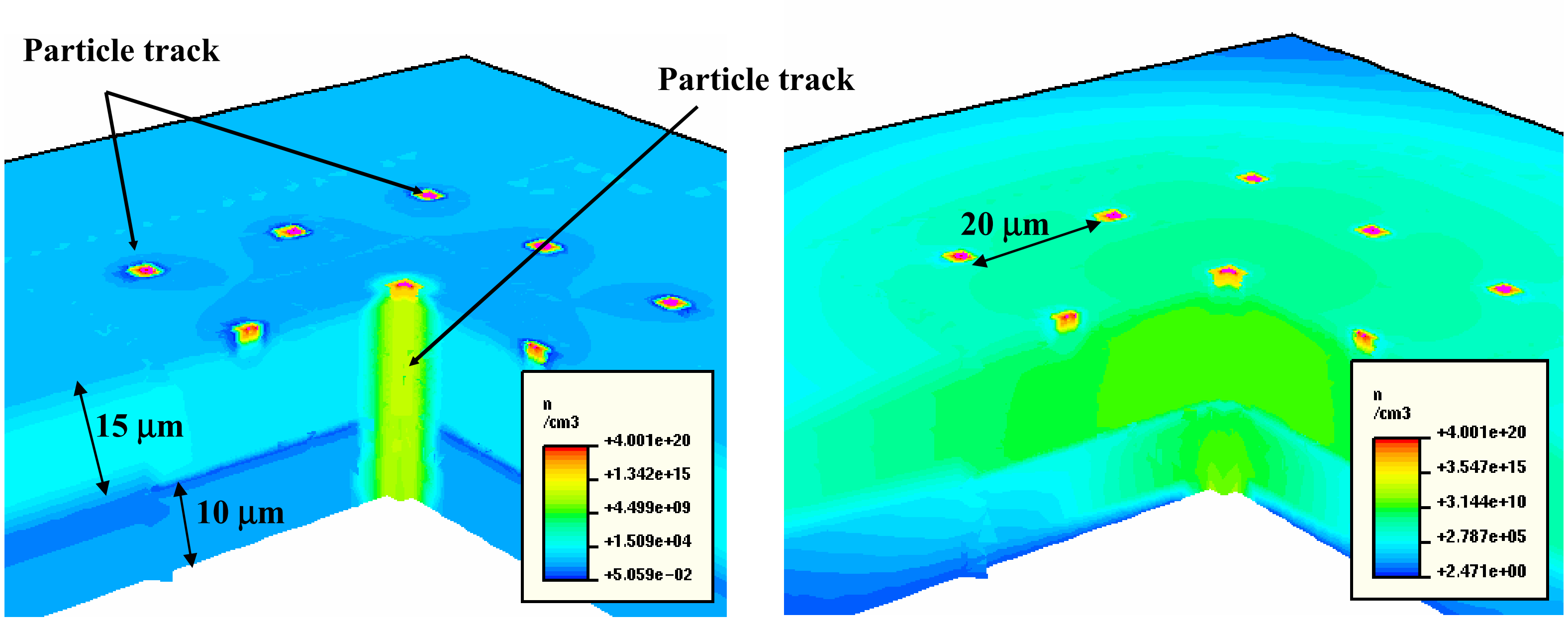
Simulation of physics process



$\tau = 0$ ns Carrier concentration $\tau = 25$ ns

- The charge collection efficiency examined using the mixed mode device and circuit simulator DESSIS-ISE from the ISE-TCAD package,
- The charge collection is traced as a relaxation process of achieving the equilibrium state after introducing an excess charge emulating passage of the ionising particle
- The device is described in three dimensions by a mesh generated using the analytical description of doping profiles and the boundary definition corresponding to the real device,
- Different detector parameters, including the thickness of the epitaxial layer, the size of a pixel and collecting diodes and number of diodes per pixel, were investigated.

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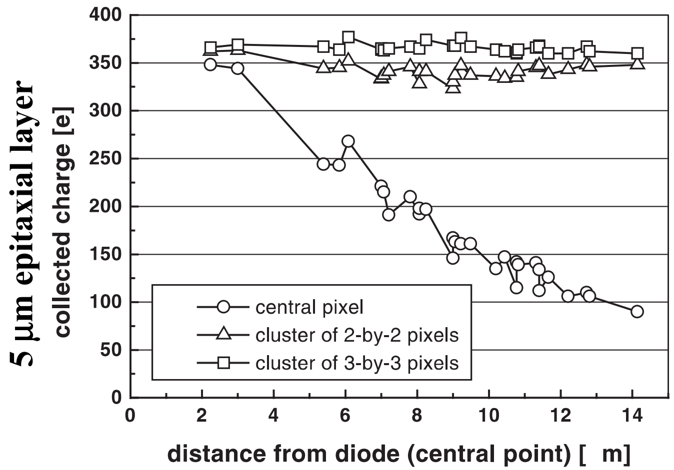
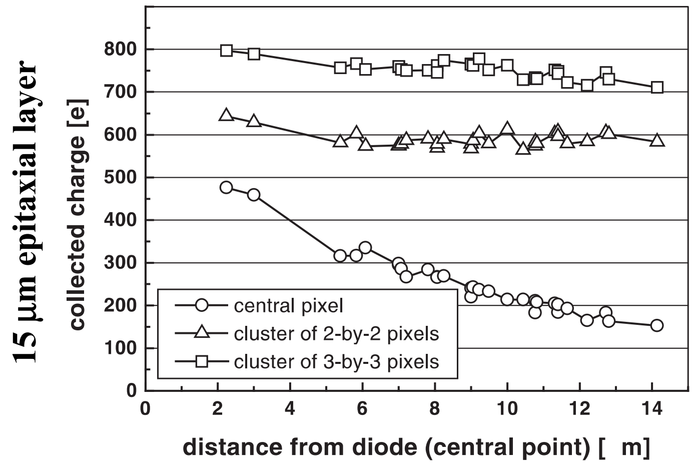
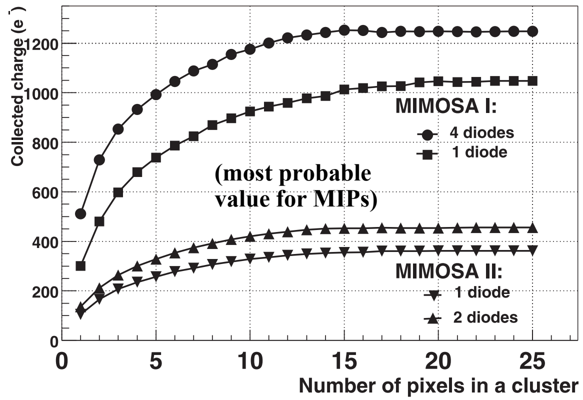
Simulation of physics process

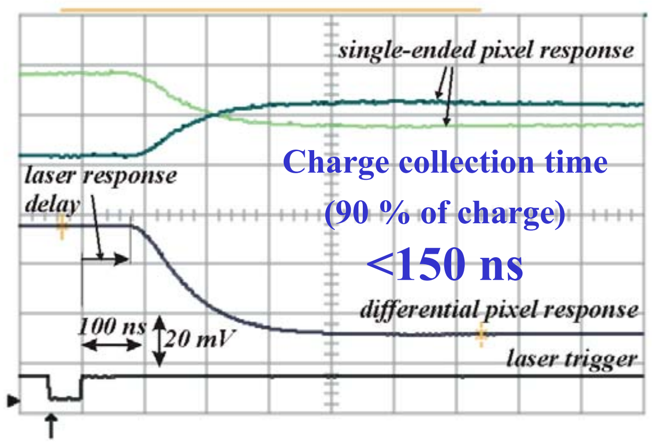




- **Experimental verification:**



The measured collected charge for two chips having 14 µm and less then 5 µm, the pitch of 20 µm



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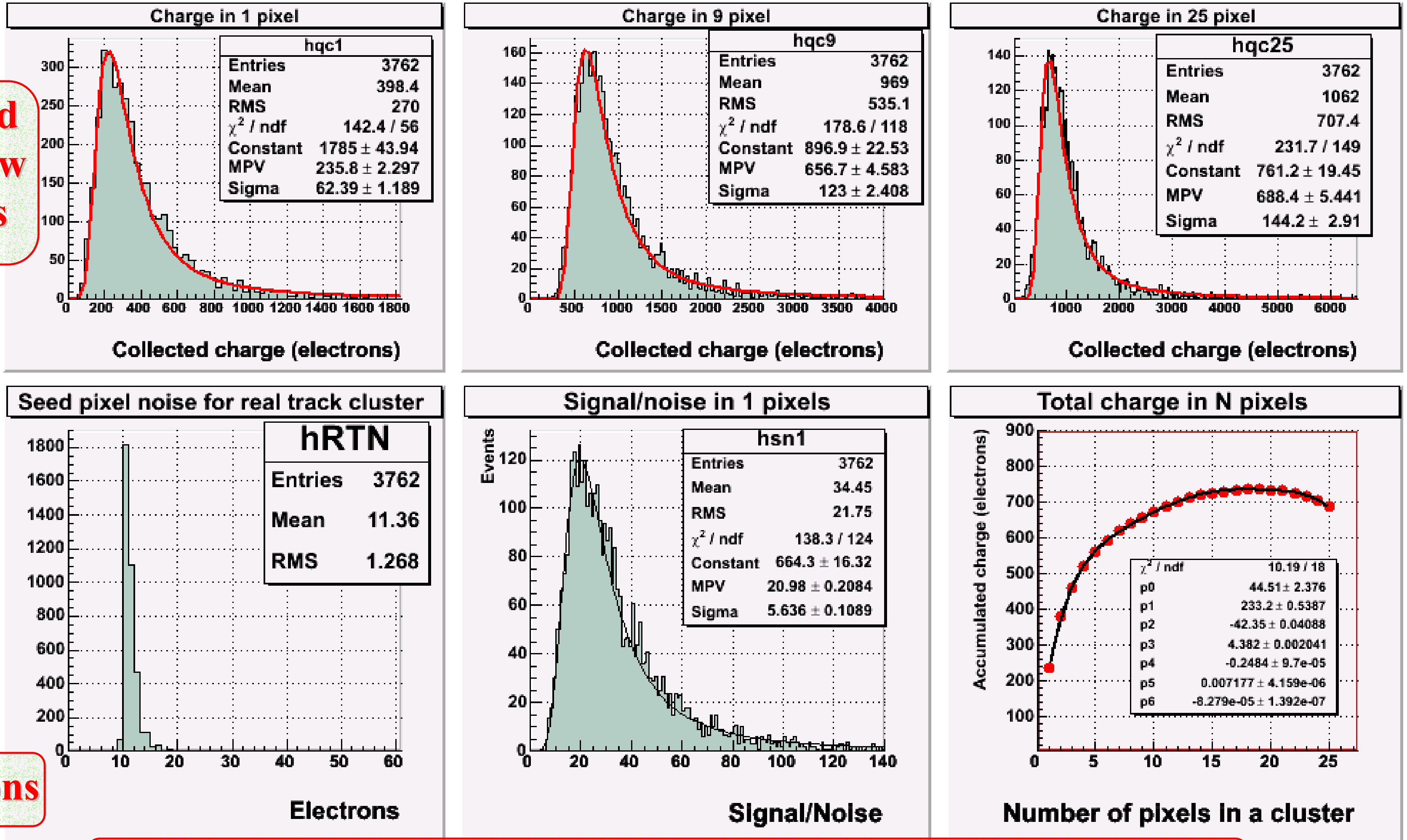
A "typical" example from the beam tests: 30µm pitch array, 20°C

M9 ; run 9534; Pl 10, dist 90; Gain 7.200; eff 99.810 +- 0.070; Seed 6.0; Neigh 4.0

Signal in the seed pixel: down to few tens of electrons



ENC: ~10 electrons

Efficiency >99%, spatial resolution: down to 1.5 µm

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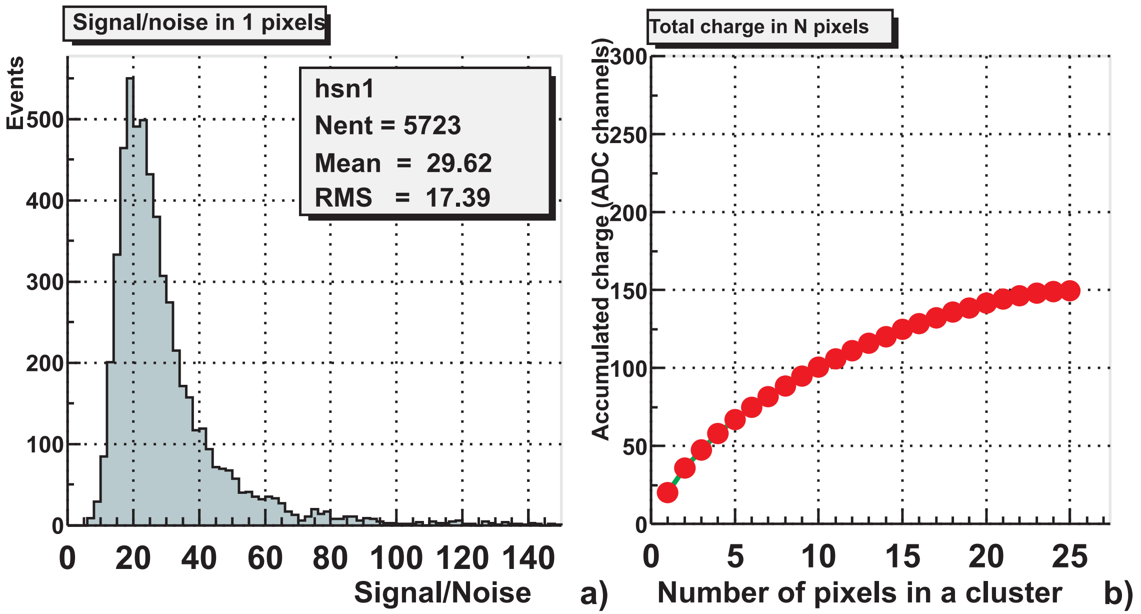
MIMOSA-4 test results:

0.35 mm AMS process without epitaxial layer
but with low doping (resistivity) substrate



Observed performances with 120 GeV/c p- at CERN-SPS:

- Detection efficiency ~99.7%
- S/N ~30 but charge is wider spread
- Spatial resolution ~4 µm (20 µm pitch)

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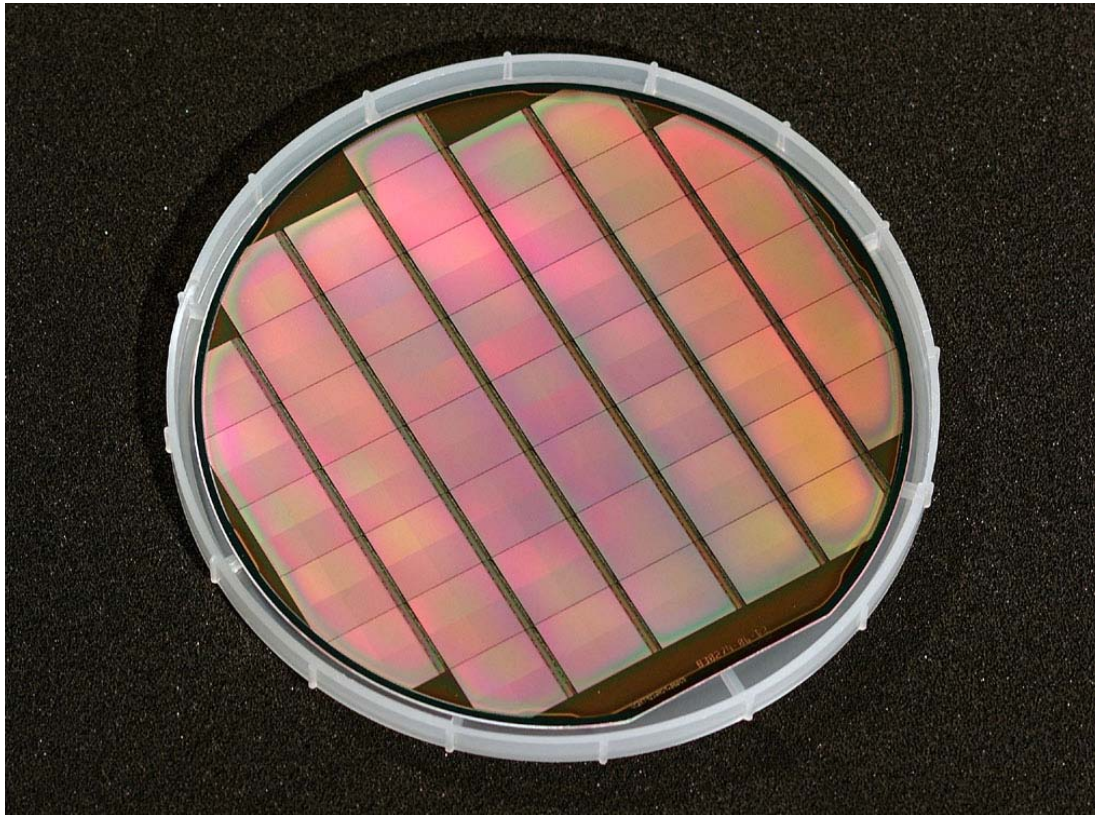
Wafer scale MAPS prototype example: Mimosa5 (10^6 pixels) in AMS-0.6 µm CMOS process (2003)



Six inch wafer hosts 33 sensors, 1.7×1.9 cm^2 each

Maximum allowed size of a circuit in a standard CMOS process: ~20x20 mm^2 (reticle)

Reticle stitching is needed, in order to get a larger device (a ladder, ~10x2 cm^2)

MIMOSA5

Each reticle is an independent circuit. Periphery logic and bonding pads layout along one side. Simplified stitching of up to 7 reticles in one direction. Still some problems with a yield (~30-40%) but it can be solved (according to some digital imager suppliers).

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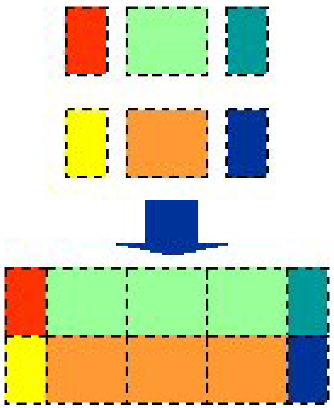
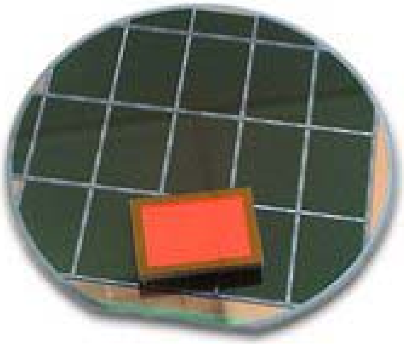
Real stitching, as offered by TOWER Semiconductor Ltd. The way to fabricate monolithic ladders?





Kodak Professional 14 Mpixel Camera

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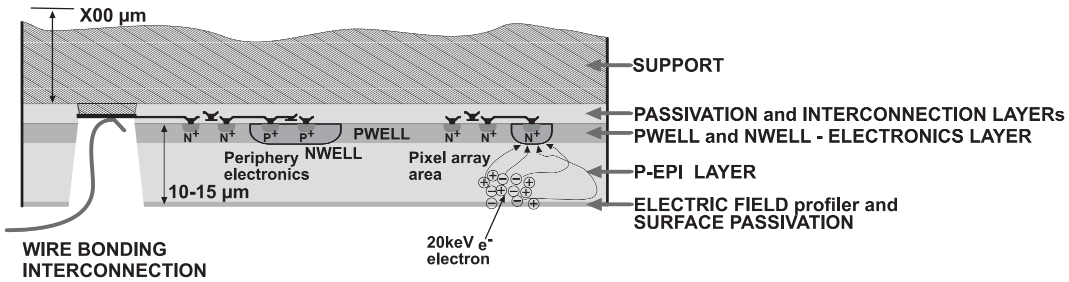
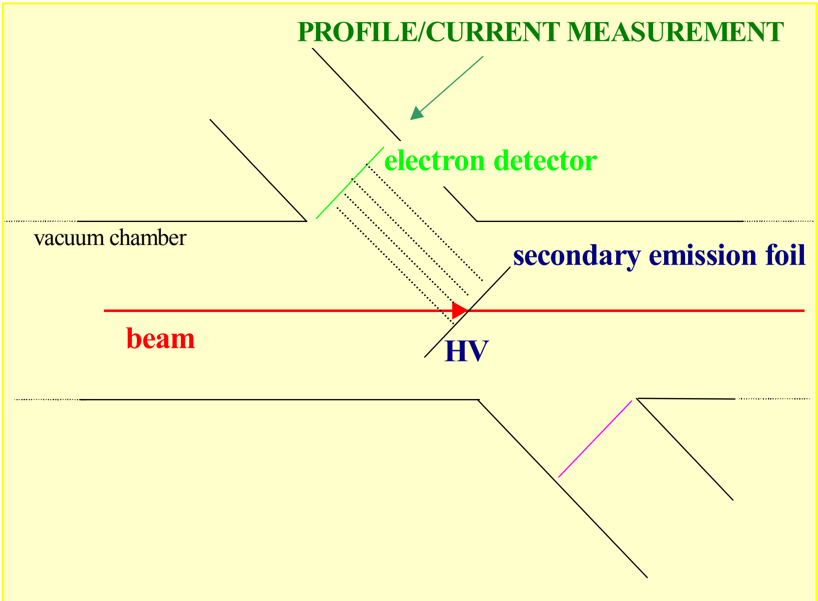
Thinned and back-side illuminated MAPS for low energy electrons imaging. SUCIMA Collaboration development for SLIM application





→ **See G. Deptuch contribution**

SLIM ≡ Secondary Emission for Low Interception Monitoring: non-destructive beam monitor

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Number of application: HPD active element (single photon imaging), tritium autoradiography and others

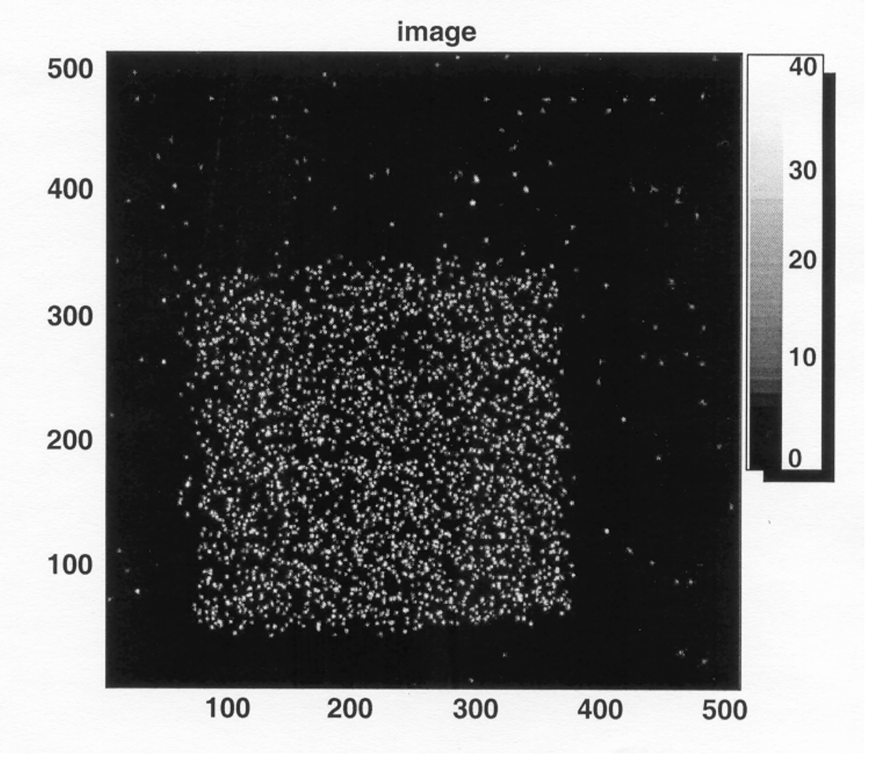

Image of a tritium source

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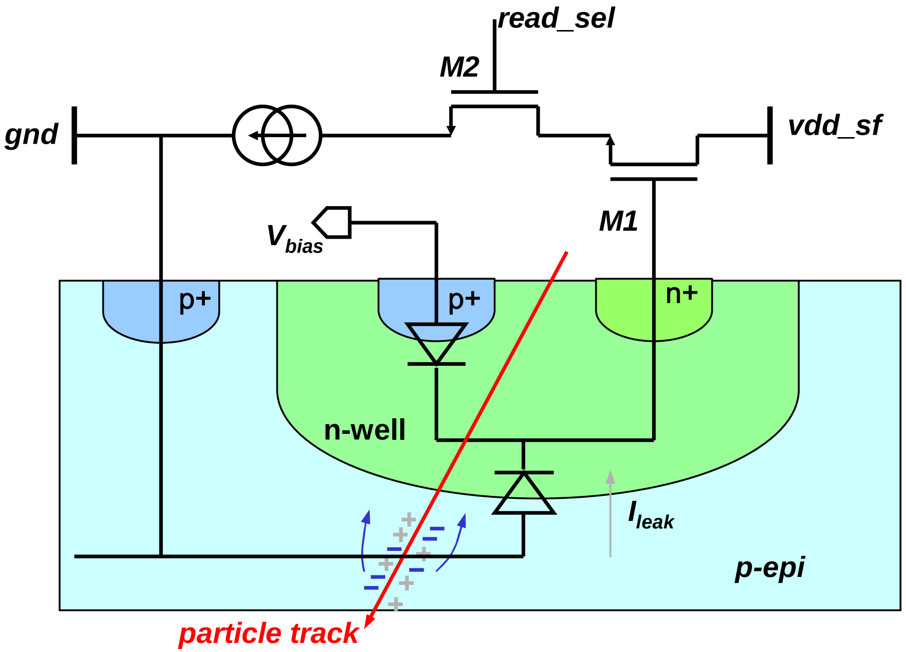
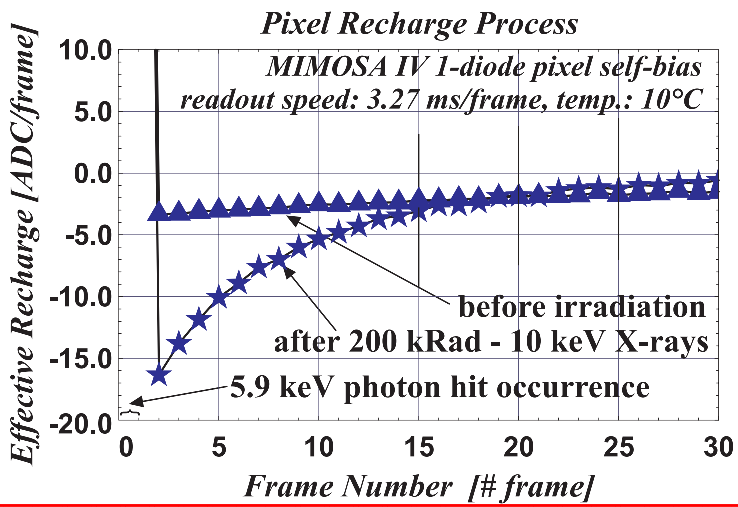
Modified sensing elements: self-biasing diode



DC level stabilization

RESET transistor replaced by a forward-biased diode, equivalent of a ~TeraOhm resistor for a ~fA (typical) leakage current



Typical RC constant: tens of ms (even after irradiation)

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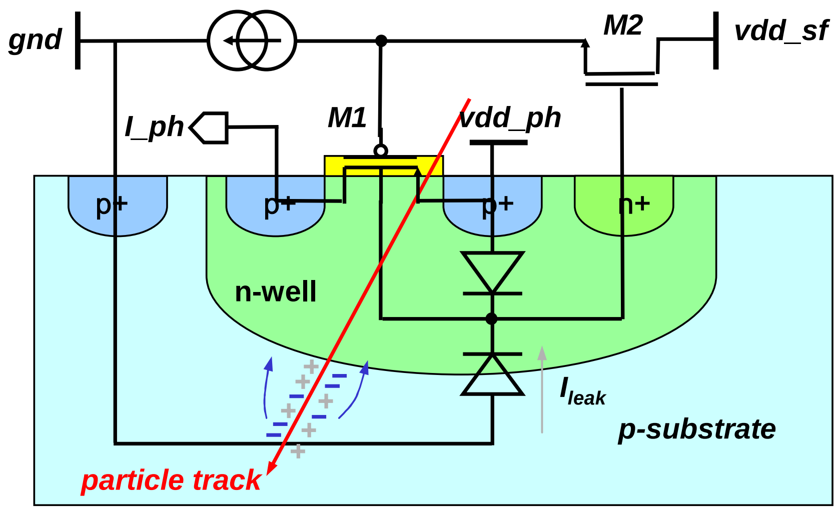
New charge sensing elements: PhotoFET



Charge collected at the N-well affect the threshold voltage of a pMOS transistor and modulates its current: signal amplification

-Charge-to current amplification

-High transconductance = high sensitivity

-Low noise/large collection area

First prototype test results

Sensitivity: 330 pA/electron

ENC: ~5 electrons

But serious (and confirmed) performance degradation when assembled in array… Substrate pick-up???

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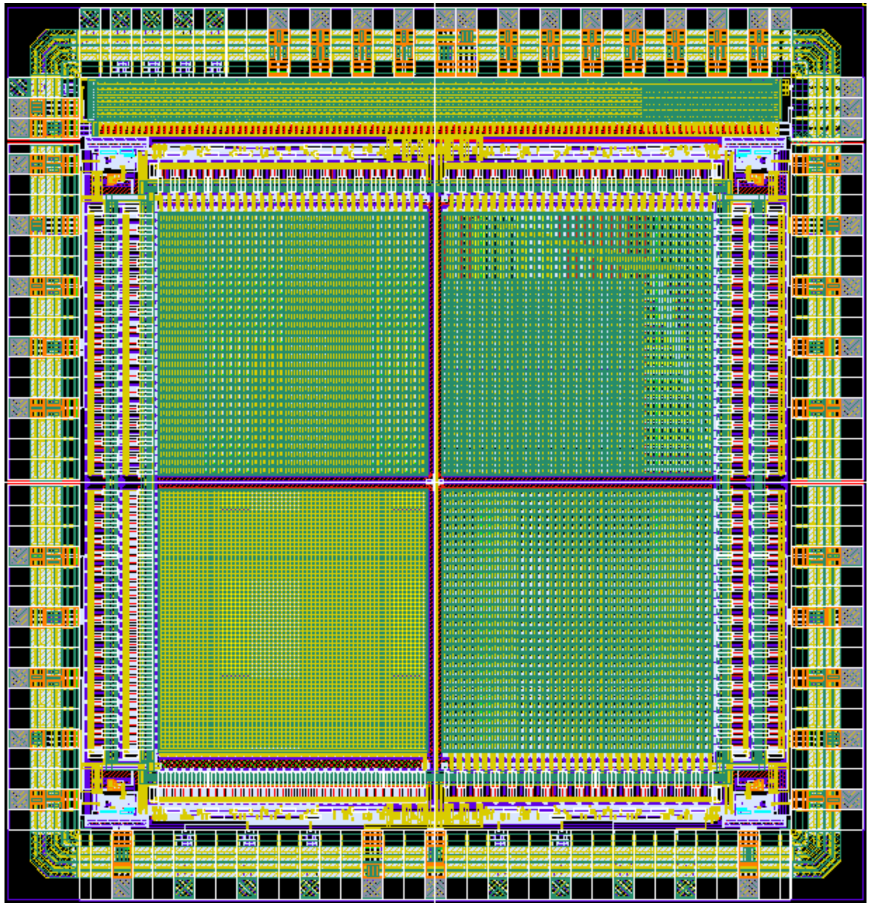
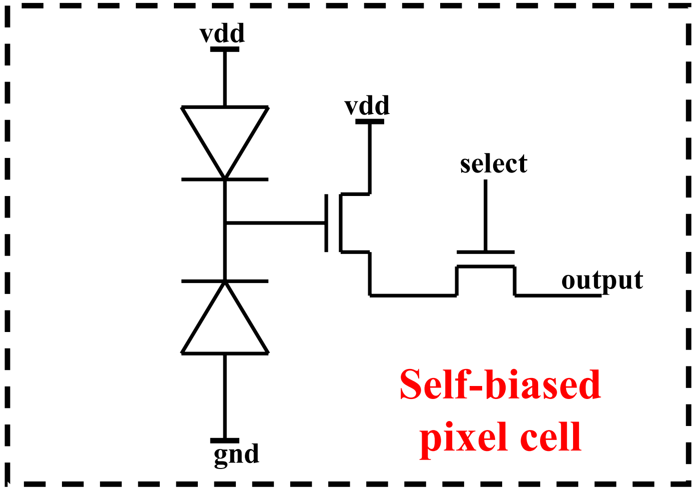
Small scale prototype MIMOSA9: "self-bias" arrays with various pitch for tracking study



Dimensions: 4.1x4.3 mm²

AMS 0.35 µm CMOS OPTO process

- Advanced mixed-signal polycide gate CMOS: 4 metal, 2 poly, high-res poly, 3.3V and 5V gates
- Optimized N-well diode leakage current
- 14 µm epi substrate (20 µm possible)
- Availability through multi-project submissions, with a reasonable pricing



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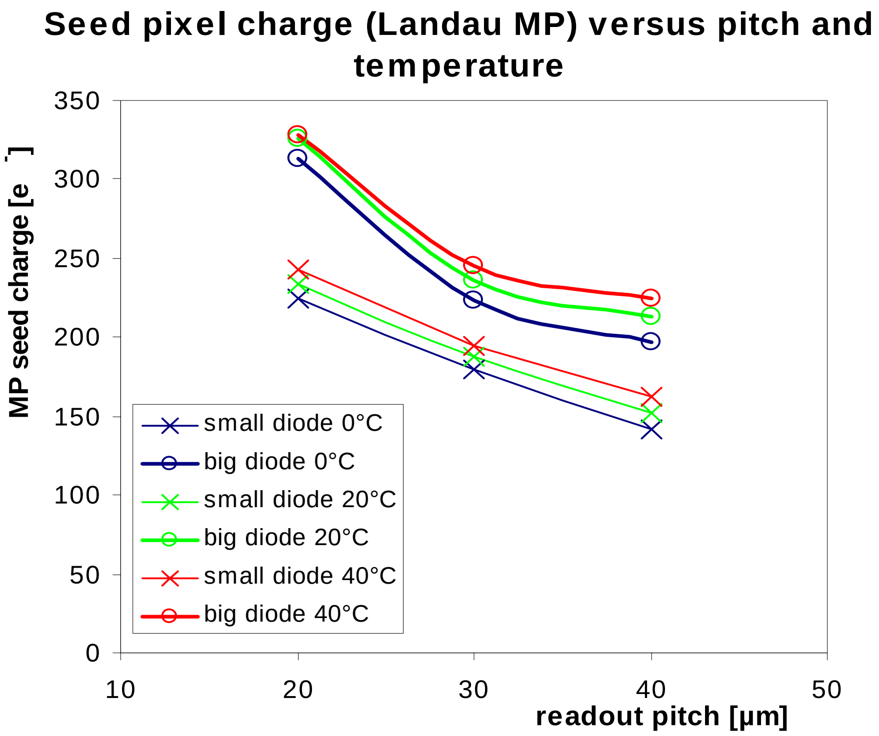
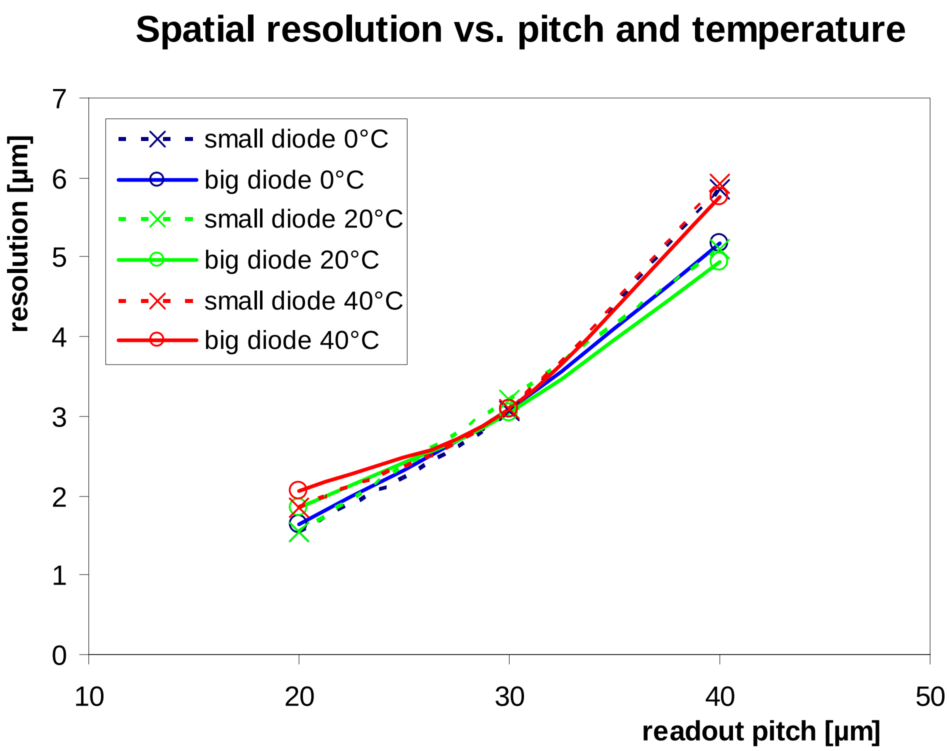
Mimosa9 beam tests: charge collection and spatial resolution





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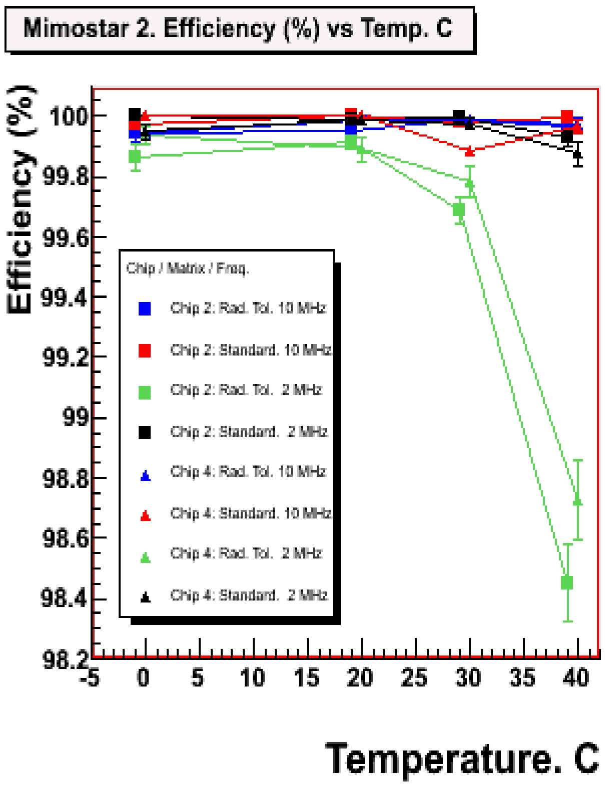
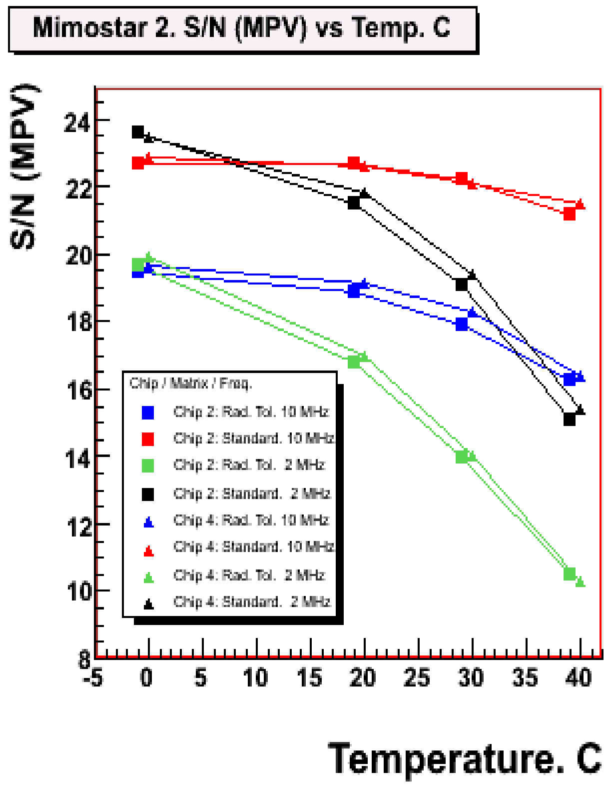
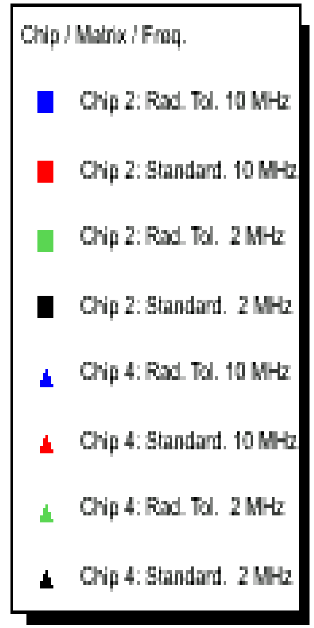
Mimo*2 (Mimosa14): the demonstrator for STAR experiment microvertex upgrade. Based on radiation tolerant N-well collecting diodes. JTAG based control and bias setting







Efficiency >99.9 % at room temperature AND long (4ms) integration time, for the seed S/N cuts of 5 (fake hits rate $<10^{-5}$)

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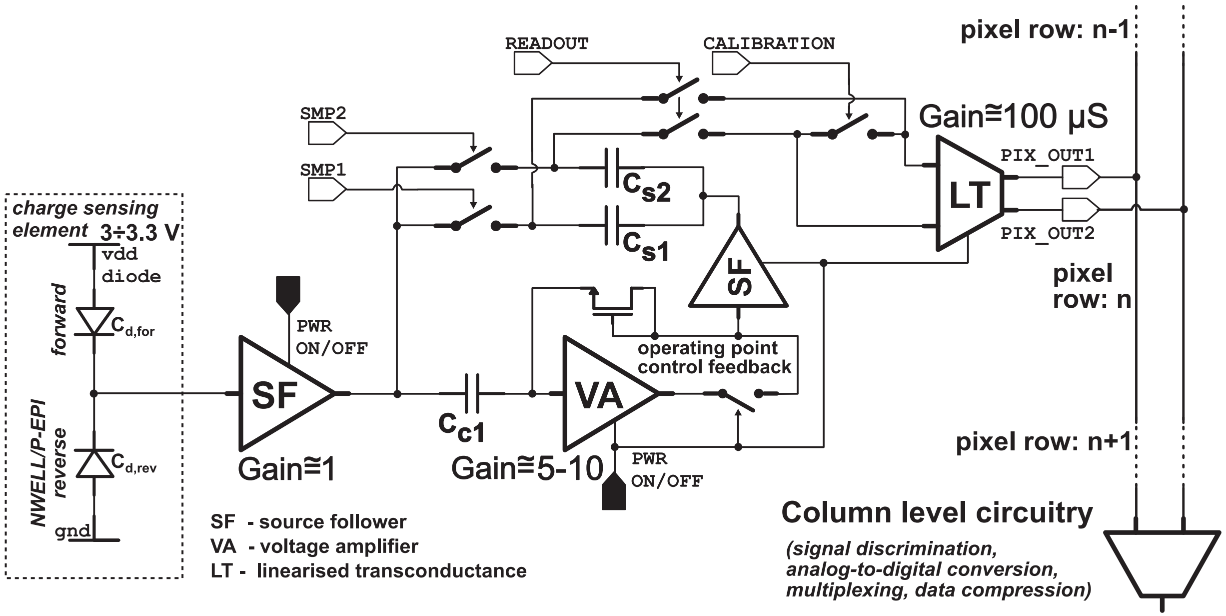
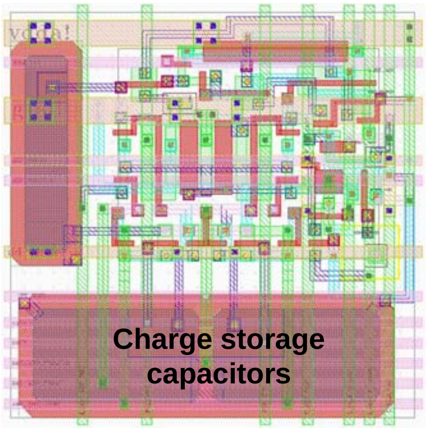
MIMOSA-6: first sensor with integrated functionality IReS-LEPSI/DAPNIA collaboration



Amplification (x5.5), AC coupling, analog memory (2 cells), <u>on-pixel CDS</u>, current output buffer, <u>discriminator per column</u>

128 pixels/column, 5MHz effective readout frequency, Power dissipation ~500 µW/column



Pixel layout: 28x28 μm^2 29 transistors

<u>First results:</u>

ENC = 15 electrons
Comparator offset (input referred) < 1mV
Pixel-to-pixel output voltage dispersion too high!

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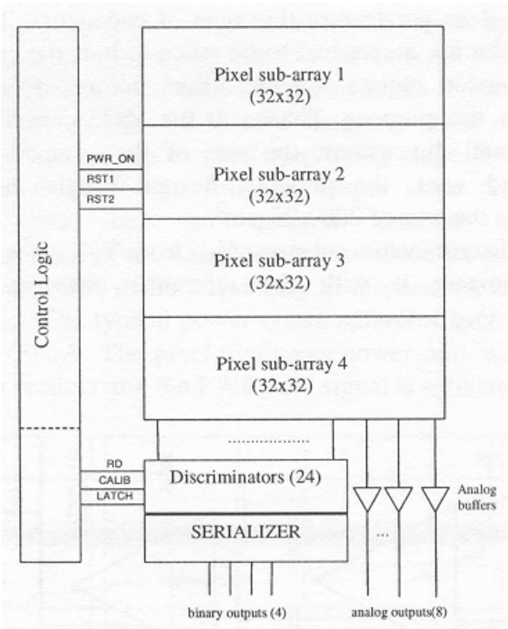
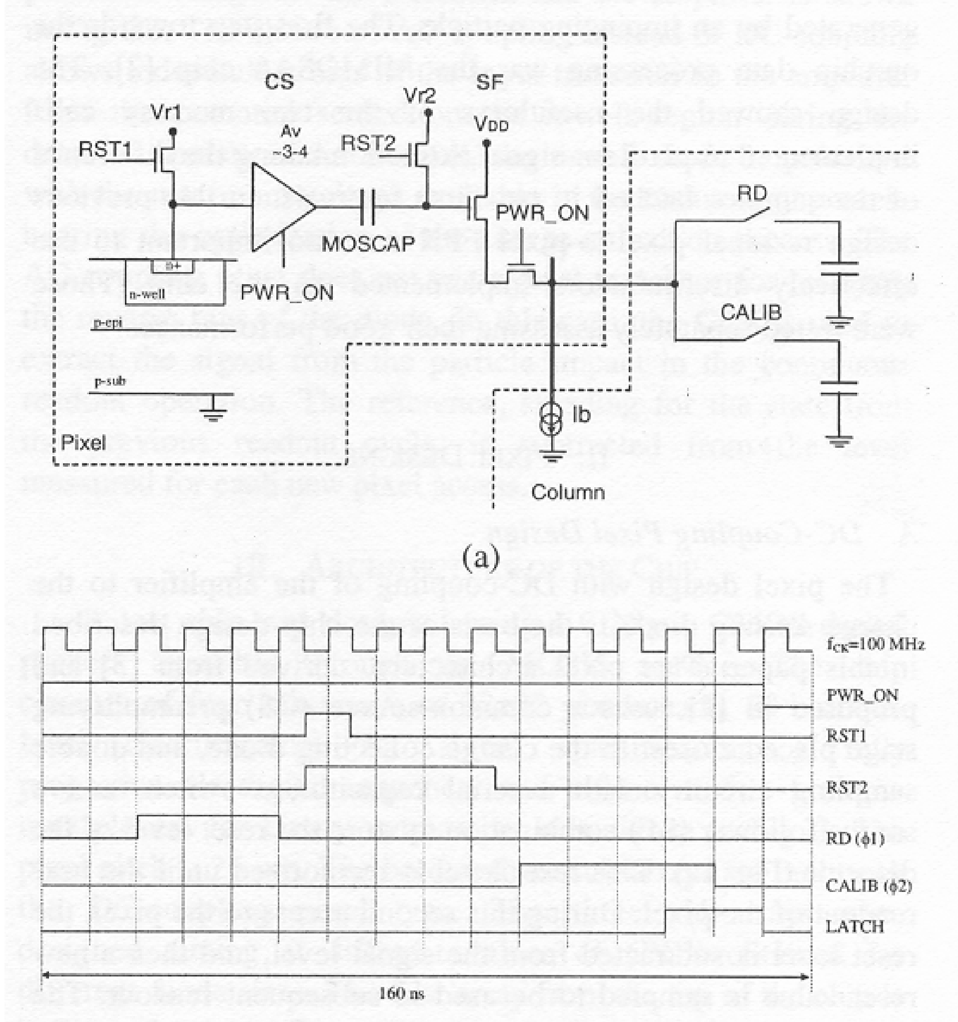
Mimosa8 (TSMC-0.25μ, 8 μm epi) – a binary readout demonstrator

- Clamping based CDS in pixel
- On-chip FPN suppression
- On-chip discrimination
- Pixel pitch 25 x 25 μm2



Prototype in collaboration with Dapnia/Saclay



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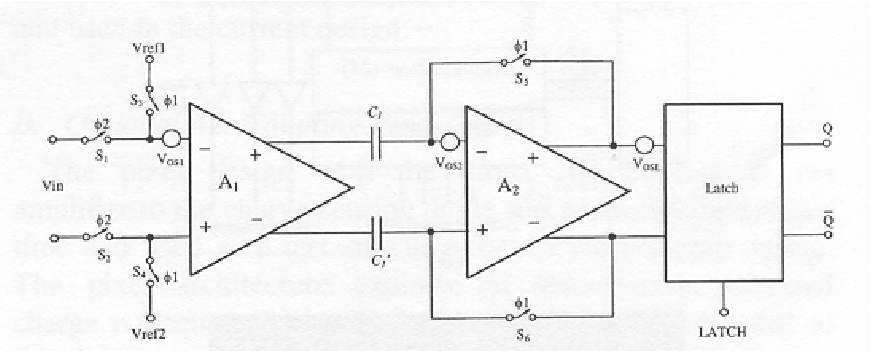
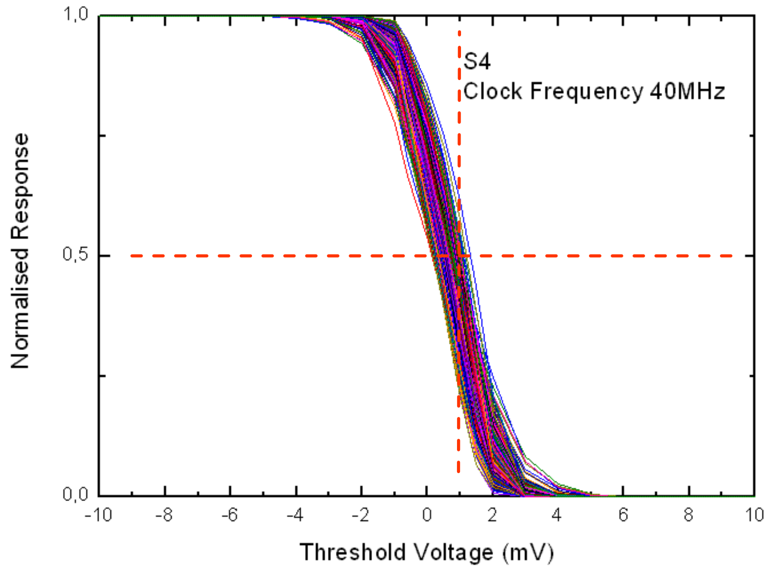
Mimosa8 (TSMC-0.25µ, 8 µm epi) – a binary readout demonstrator



Offset compensated comparator at the end of each column



Comparator threshold voltage scan for ALL pixels (of one type)

- **Output noise: 0.9 mV (ENC = 15 electrons)**
- **Pixel-to-pixel FPN: 0.45 mV**

For more details → See Yavuz Degerli with his “back-up” poster contribution

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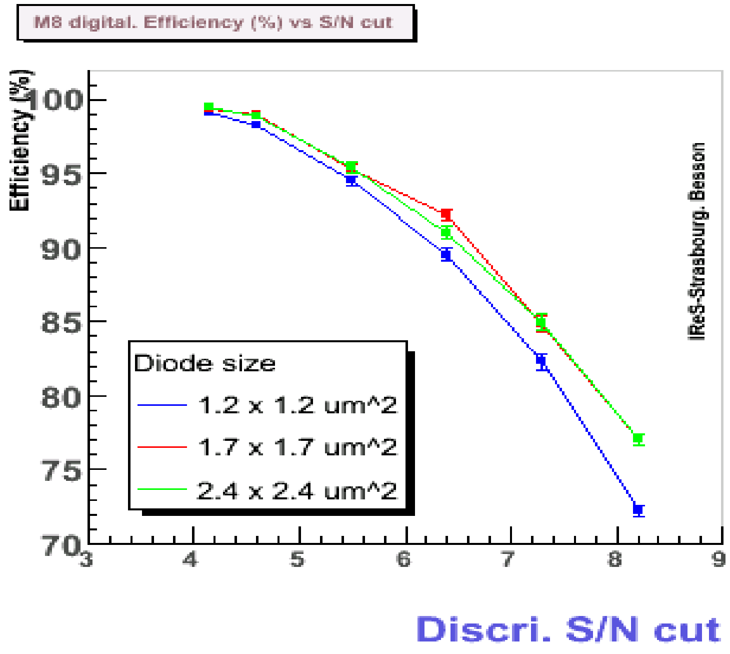
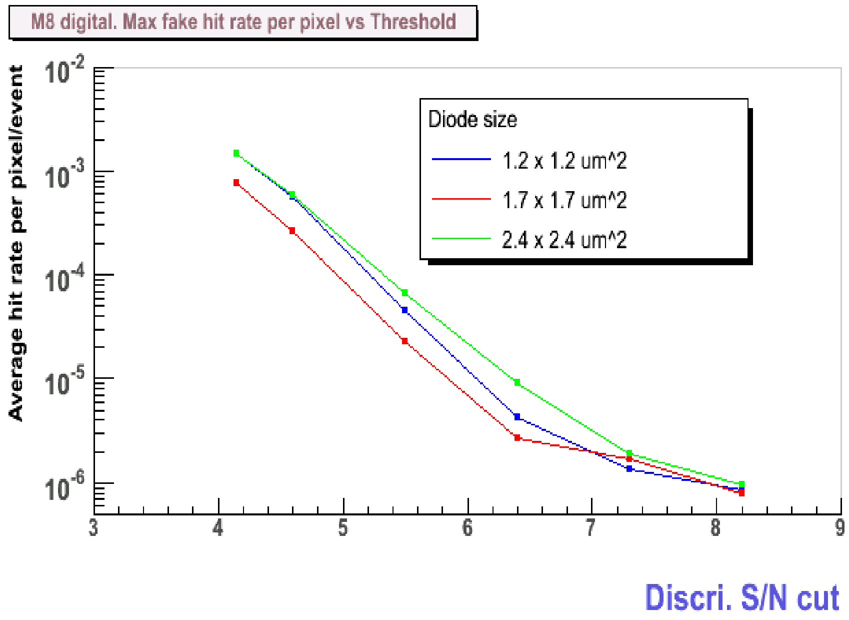
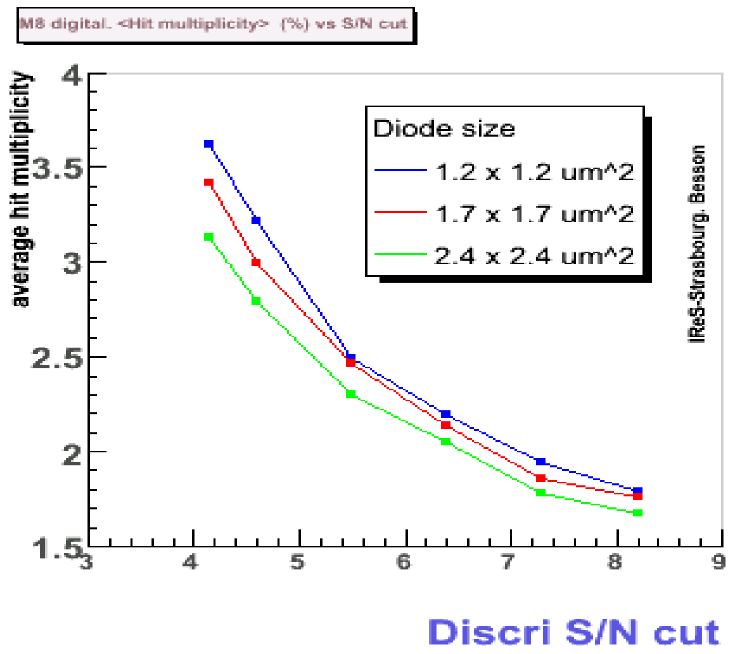
Mimosa8 beam tests results







- First demonstration of feasibility of FPN correction using on-chip real time circuitry
- The design goal confirmed by the beam tests results: efficiency > 98 %

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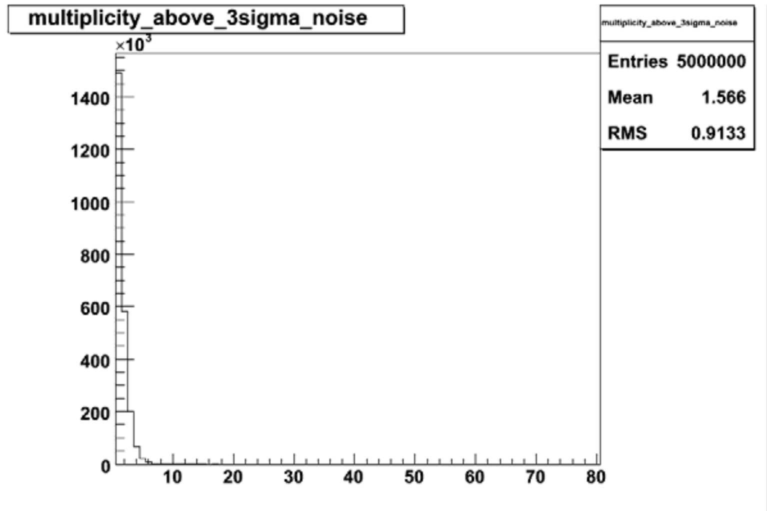
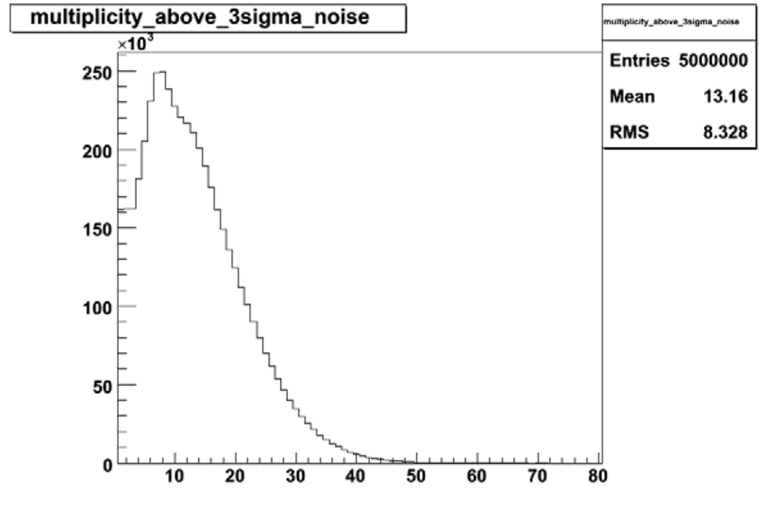
On-pixel amplifiers development → see A. Dorokhov contribution

Be careful with minimum size N-well diodes!

1.7 x 1.7 um² diode



2.4 x 2.4 um² diode



Measured cluster multiplicity

There are no hits above 3 sigma noise in case of small diode!

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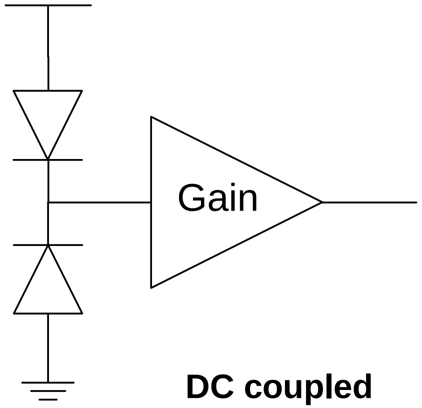
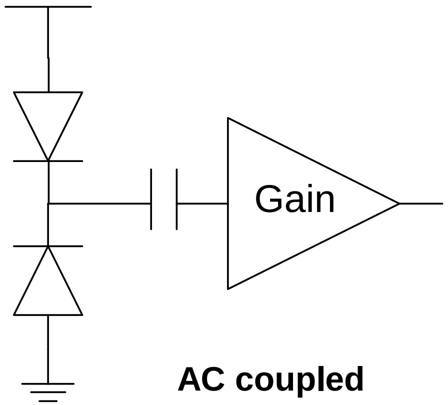
DC versus AC diode coupling



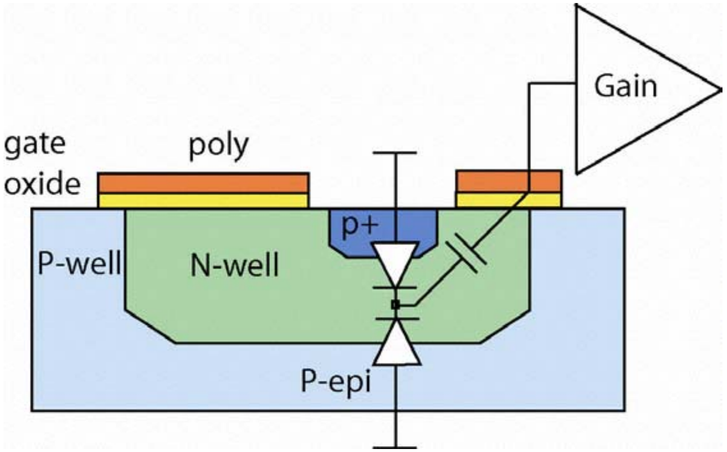
DC coupled



AC coupled

AC coupled amp:

- Separation from power supply of the sensing node
  - Increase of the voltage ⇒ increase of the depleted region ⇒ no change on the operating point of an amplifier
- But…
  - More parasitics, more complicated amplifier biasing circuitry, difficult to implement compact and stable coupling capacitor



Compact implementation

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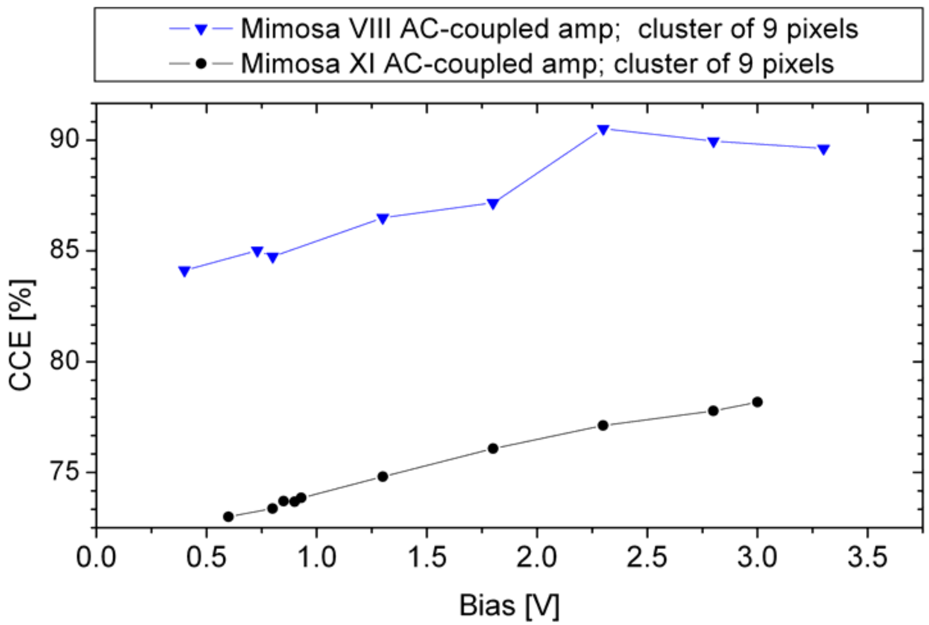
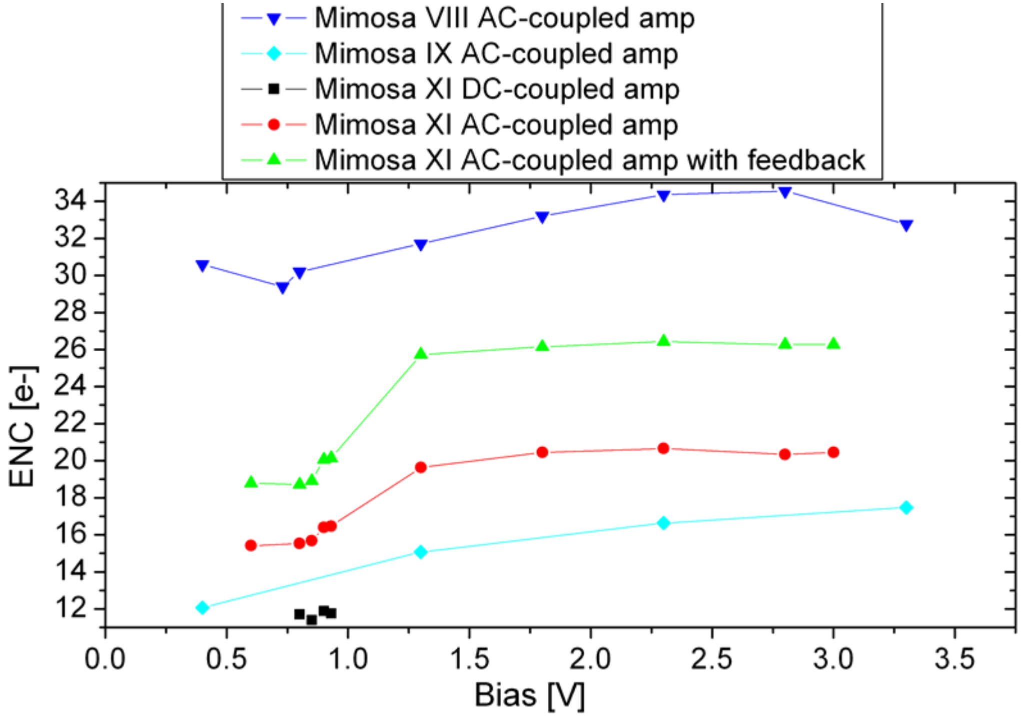
DC versus AC diode coupling

Charge collection efficiency and ENC in function of bias of charge collecting diode





DC seems to win in simplicity and performance…

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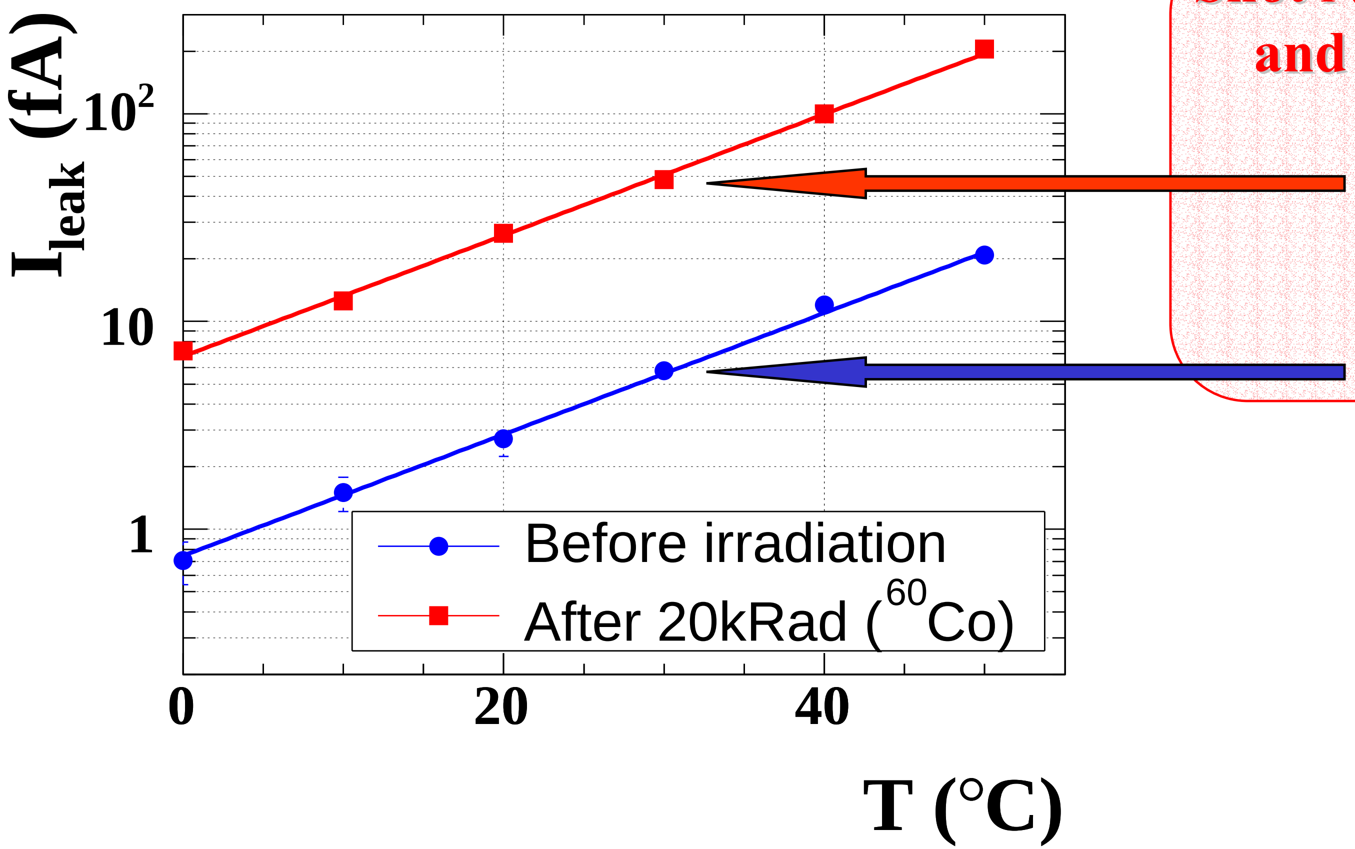
Radiation tolerance for integrated ionizing dose: dark current increase



Shot Noise Contribution @ 30°C and @4 ms integration time

ENC_{shot} = 39 electrons

ENC_{shot} = 12 electrons

Standard N-well/p-epi diode dark current increase after irradiation with a ^{60}Co γ source (Mimosa9)

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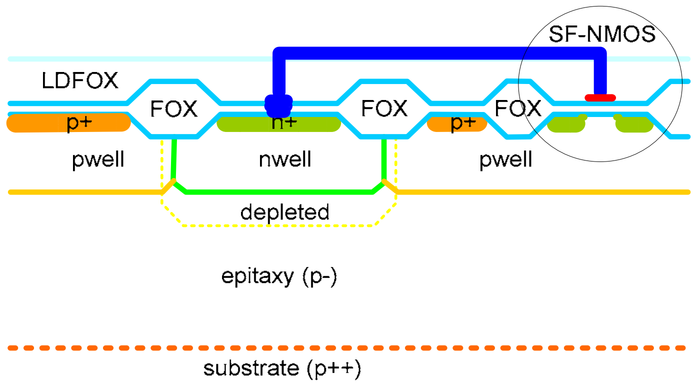
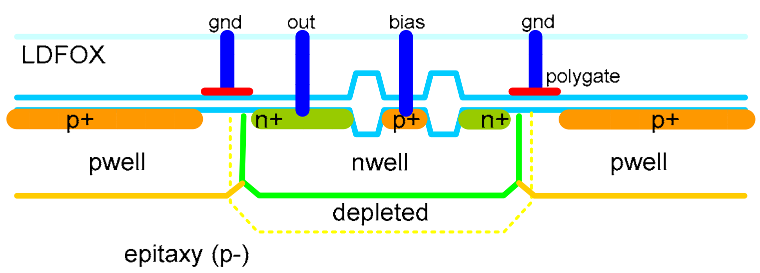
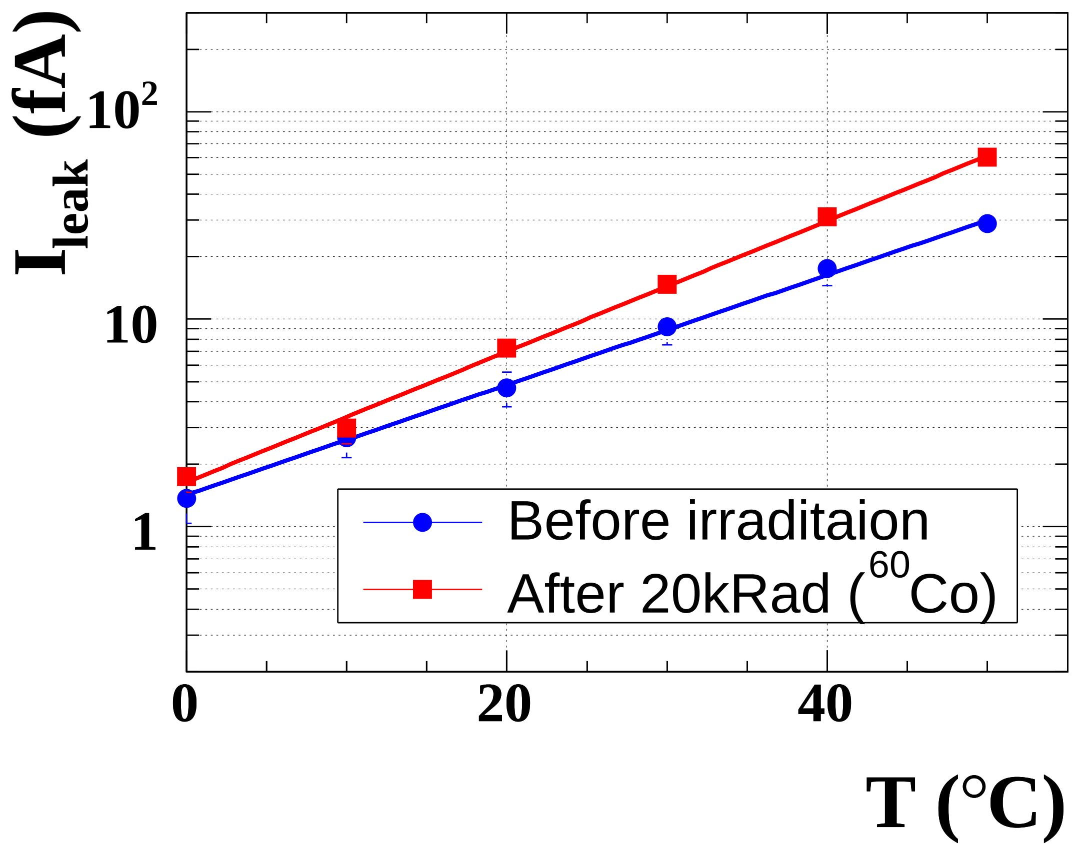
"Thin-oxide" diode dark current increase after irradiation with a ^{60}Co γ source



standard diode layout



thin-oxide diode layout



Recent results (Mimosa15): x10 current increase after 1Mrad

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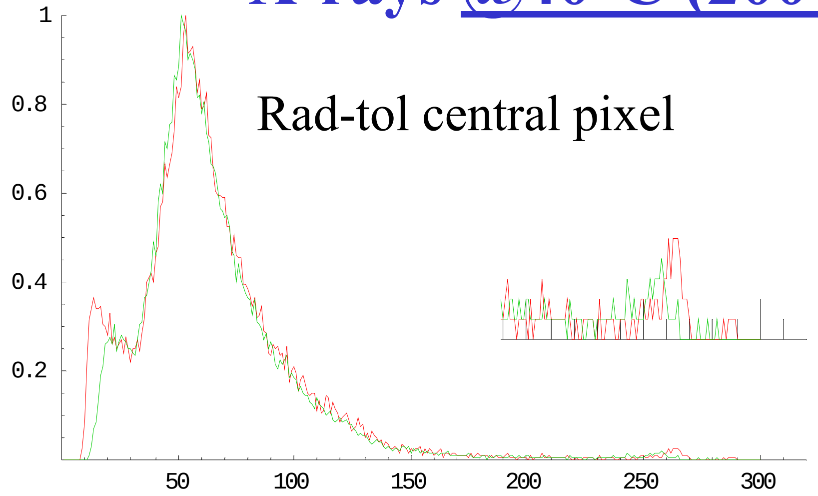
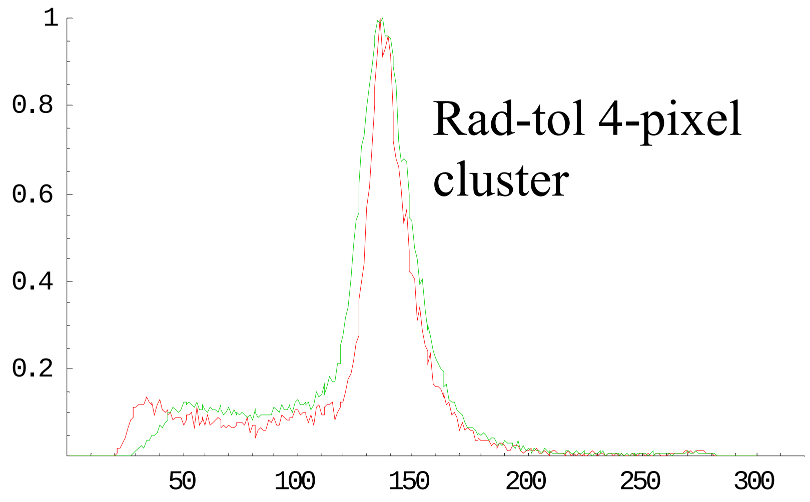
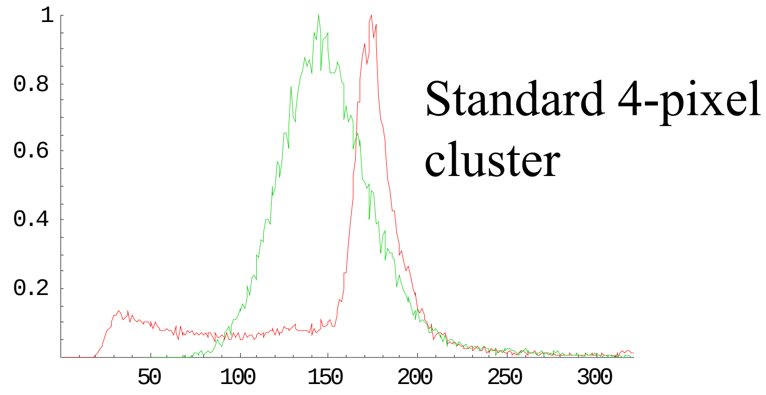
Fe^{55} spectrum before (red) and after (green) 1 Mrad of X-rays @40°C (200 µs integration)







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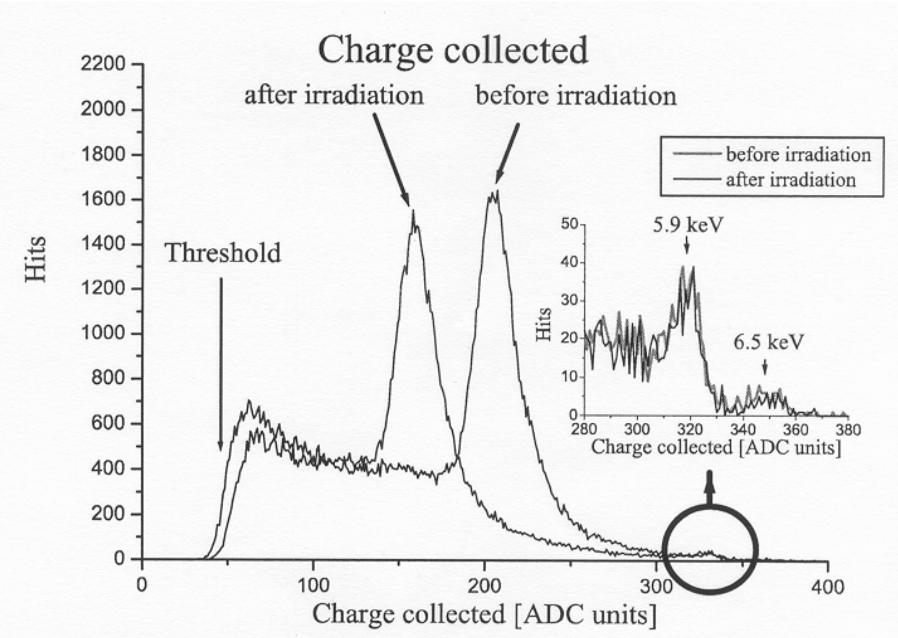
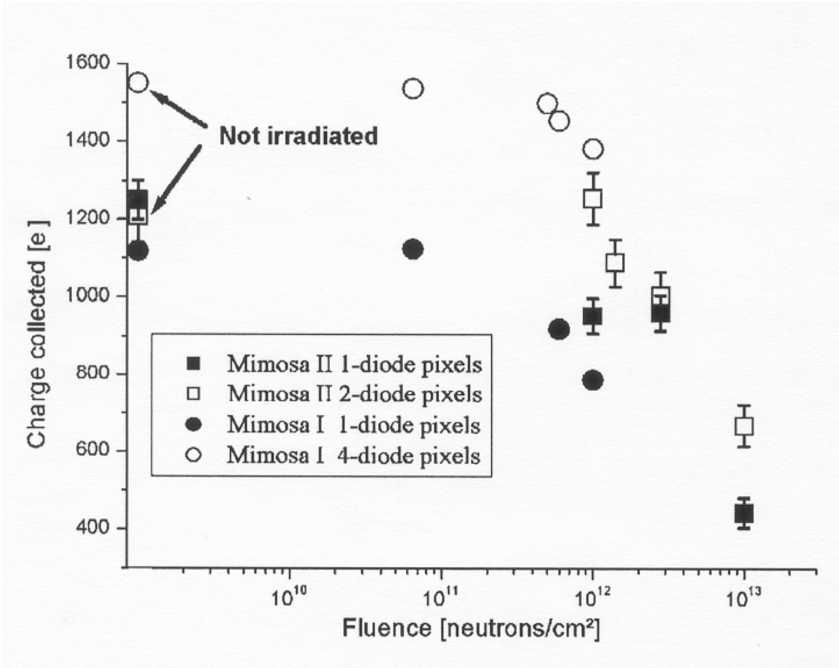
Radiation tolerance for the bulk damage: neutron irradiation





Charge loss after ~10^{12} n/cm^2, correlated to the diode/pixel area ratio, seems to be rather basic and process independent

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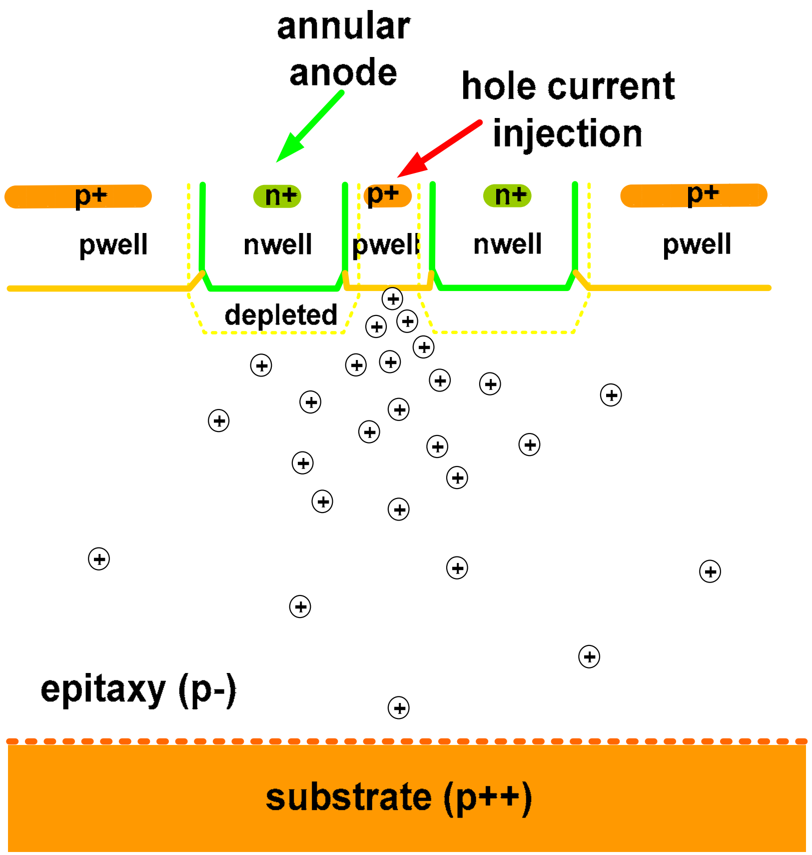
Possible improvements: P. Rehak et al. *"A novel position and time sensing Active Pixel Sensor with field-assisted electron collection for charged particle tracking and electron microscopy"* → *see Pavel's contribution*



Novel (simplified) UMAPS structure

Field shaping using injected hole current → faster charge collection → smaller sensitivity to the <u>bulk damage</u>

Field shaping → smaller charge spread → optimum conditions for the <u>binary readout</u>

No success in experimental confirmation till now…

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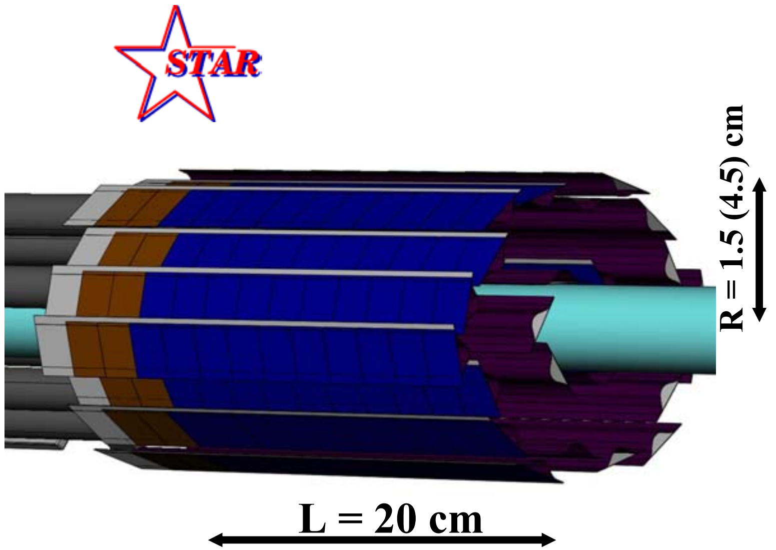
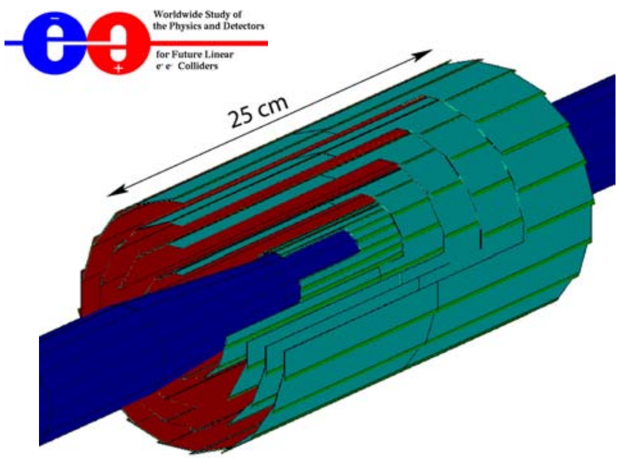
Applications of MAPS in particle physics experiments



STAR VxD upgrade 2008: 6+18 ladders

- (analog) readout time = integration time = 2 – 4 ms
- Room temperature operation (chip at ~ ≤40°C)
- Air cooling only
- Ionizing radiation dose:~8 krad/year (3 10^{11} π/cm^2/year)
- The Ultimate Upgrade: luminosity up, dose respectively higher , integration time ~10x shorter. Considered solution is based on column-parallel binary readout.



ILC VxD

- Beam train: ~1 ms every ~200 ms
- Outer layers integration time: < ~200 μs
- Inner layers integration time: < ~25 - 50 μs
- Possible option: 1 ms "train integration mode"
- Neutron eq. fluence: < ~10^{10} n_{eq}/cm^2/year
- Ionizing dose: <50 krad/year (~10 MeV electrons))

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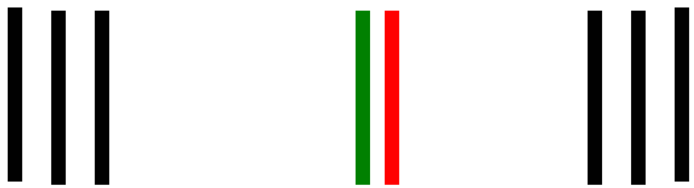
General Purpose Beam Telescope: a precision tool for testing a new generation of detectors being developed for International Linear Collider (ILC): part of EUDET program

Technical specs:

- Compact: to be mounted inside existing magnets, transportable
- User friendly, easy to run AND <u>to interface with various users</u>
- <u>Sensitive area: few sq. cm, (at least 2 cm in one direction)</u>
- <u>High precision tracking: down to 2 µm (or better) in the center, also at medium energy (6 GeV) electron beam at DESY</u>



High-precision configuration layout: the distance DUT-reference plane ~ 1 mm

Standard tracking plane (3 µm resolution) — black

Optional high-precision plane (1 µm resolution) — red

Device under test (DUT) — green

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Conclusions

MAPS development at Strasbourg is a continuous fun since seven years!

However, first real applications are expected soon and will critically verify our enthusiasm for this devices …

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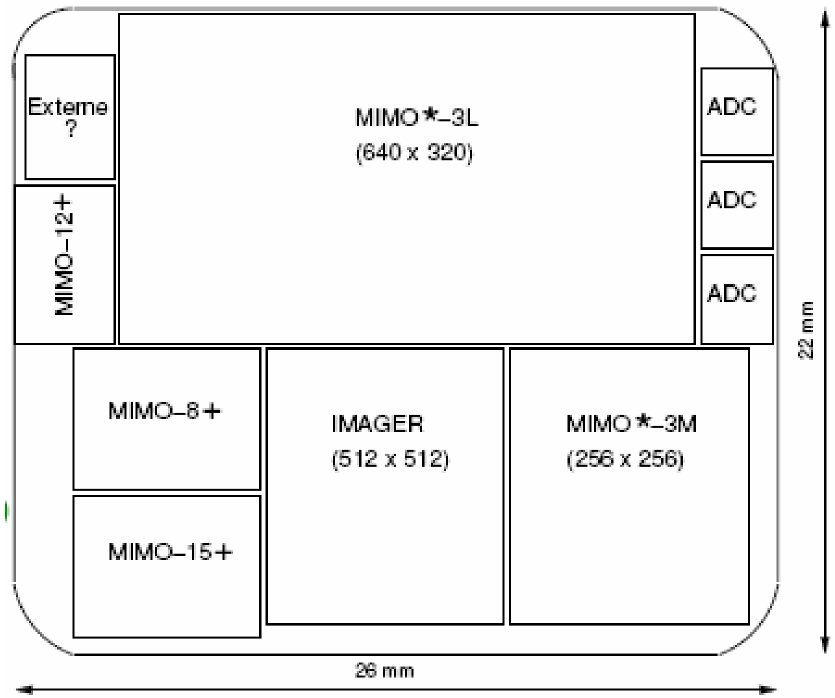
Sensor fabrications in 2006

- Engineering Run in AMS 0.35 OPTO (end June 06)
  - **Motivated by MIMOSTAR-3L :**
    - 200 kpixels, $t_{r.o.}$ = 2 ms, 2 cm^2
  - **Other chips:**
  - ➢ MIMOSTAR-3M: 0.8x0.8 cm^2, rad.tol., 800 µs (EUDET)
  - ➢ MIMOSA-8+: binary readout architecture (EUDET, ILC)
  - ➢ MIMOSA-15+: Noise reduction, etc. (EUDET, ILC)
  - ➢ IMAGER: resolution ~1 µm (EUDET)
  - ➢ Low resolution, low power ADCs
  - **Epitaxy thickness 14 or/and 20 µm ?**



- Other submissions
  - prototype exploring a new technology: < 0.18 µm