Adapting CMOS Sensors to Future Vertex Detectors

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OUTLINE

- Remarks on experimental trends $\leftrightarrow$ Limits of existing devices for flavour tagging
- The solution of CMOS sensors:
  $\leftrightarrow$ Principle of operation – Advantages & Concerns – R&D directions – Typical performances
- Tracking detector applications foreseen: decided or ambitionned
- Current R&D frontier: signal processing architectures – radiation tolerance
- Summary
WHAT IS DRIVING THE R&D ON CMOS SENSORS?
Flavour tagging takes growing importance in understanding the dynamics underlying heavy ion and particle physics phenomena \(\leftrightarrow b, c, \tau\) tagging with **High Efficiency & Purity**!

**Ex: ILC physics programme** \(\leftrightarrow\) high performance flavour identification is a MUST for most events:

- **b, c, \tau** contained in most final states:
  
  \[t \rightarrow Wb; W \rightarrow c\bar{s}; Z \rightarrow b\bar{b}, c\bar{c}, \tau\tau; \quad \chi^\pm \rightarrow W^\pm \chi^0; \quad \chi^0_2 \rightarrow Z \chi^0_1;\]

  \(\leftrightarrow\) use b, c, \(\tau\) decays of Z and W bosons to enhance sensitivity to new physics:

  - background rejection \(\rightarrow\) measurements of \(B_r(H, X), A_{FB}, A_{LR}, \text{etc.}\)

- assign EACH track to its vertex origin (1\(^r\)y, 2\(^r\)y, 3\(^r\)y) in a POLY-JET environnement (\(Q_{Vx}, E_{flow}\))

  and establish links between 2\(^r\)y and 3\(^r\)y vertices \(\rightarrow\) reconstruct decay chains:

  
  \[e^+ e^- \rightarrow t\bar{t} \rightarrow b\bar{b}WW \rightarrow \geq 6\text{ jets}\]

  \[e^+ e^- \rightarrow t\bar{t}H \rightarrow b\bar{b}b\bar{b}WW \rightarrow \geq 8\text{ jets}\]

  \[e^+ e^- \rightarrow HA \rightarrow tttt \rightarrow b\bar{b}b\bar{b}WWWW \rightarrow \geq 12\text{ jets}\]
Aim for an ultra-light, very granular, poly-layer Vertex Detector installed very close to the interaction point

Demanding running conditions (occupancy, radiation) !!!

Existing technologies are not adequate:

- CCD (SLD): granular and thin BUT too slow and radiation soft
- Hybrid Pixel Sensors (Tevatron, LHC): fast and radiation hard BUT not granular and thin enough

CMOS sensors are expected to provide an attractive trade-off between granularity, material budget, radiation tolerance and speed
PRINCIPLE OF OPERATION
AND SPECIFIC FEATURES
OF CMOS SENSORS
Main Features and Advantages of CMOS Sensors

- **p-type low-resistivity Si hosting n-type "charge collectors"**
  - signal created in epitaxial layer (low doping):
    $Q \sim 80 \text{ e-h/\mu m} \leftrightarrow \text{signal } \lesssim 1000 \text{ e}^-$
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode with help of reflection on boundaries with p-well and substrate (high doping)

- **Specific advantages of CMOS sensors:**
  - Signal processing \( \mu \)circuits integrated on sensor substrate (system-on-chip) \( \leftrightarrow \) compact, flexible
  - Sensitive volume (\( \sim \) epitaxial layer) is \( \sim 10–15 \mu \text{m} \) thick \( \rightarrow \) thinning to \( \lesssim 30 \mu \text{m} \) permitted
  - Standard, massive production, fabrication technology \( \rightarrow \) cheap, fast turn-over
  - As granular and thin as CCDs, BUT faster and more radiation tolerant
Basic Read-Out Architecture

Based on 3 transistor cell

V_Q_integr

Vreset

\[ \Delta V_{\text{typ}} \propto I_{\text{leak}} \]

\[ \Delta V_{\text{sig}} \propto Q_{\text{signal}} \]

Integration time

t_{fr1}

t_{fr2}

Array of pixels

Pixel

Pixel Array: Column select – ganged row read

High-speed read-out

Analog read-out & storage

Low power – only significant draw at readout edge
Two different ways of reading out the sensor:

- **Rolling Shutter mode (see below):** array is read out row after row
  - each row is slightly shifted in time w.r.t. previous ones

- **Snap-shot mode (rather suited to imaging):** all rows read out at once
  - dead time before/during pulsing all rows and during read-out
Main R&D Directions

- High r.-o. speed, low noise, low power dissip., highly integrated signal processing architecture:
  - analog part (charge collection, pre-amp, CDS, ...) inside pixel
  - mixed (ADC) and digital (sparsification) micro-circuits integrated inside pixel or aside of active surface

- Optimal fabrication process:
  - epitaxial layer thickness
  - (dark current)
  - number of metal layers
  - cost
  - yield
  - life time of process

- Radiation Tolerance:
  - dark current
  - doping profile
  - (latch-up)

- Room temperature operation:
  - minimise cooling requirements
  - performances after irradiation

- Industrial thinning procedure:
  - minimal thickness
  - individual chips rather than wafers
  - yield
M.I.P. TRACKING PERFORMANCES:

PIXEL & CLUSTER CHARACTERISTICS,

DETECTION EFFICIENCY
Several groups design CMOS sensors for charged particle tracking:

- **BELLE upgrade → SuperBELLE:**
  - Univ.Hawai

- **STAR upgrades:**
  - IReS/IPHC (Strasbourg)

- **ILC (EUDET C E.U. FP-6):**
  - IReS/IPHC (Strasbourg), DAPNIA (Saclay), LPC (Clermont), LPSC (Grenoble), Univ.Roma-3, Univ.Bergamo, Univ. Pisa, RAL, LBL, BNL, Univ.Oregon & Yale (SARNOF)
  - others (?)

- **CBM (GSI):**
  - IReS/IPHC (Strasbourg)

Several other groups involved in chip characterisation & detector integration issues

**R&D for Super BELLE:** hits in 1st beam telescope made of 4 CAP-2 sensors exposed to 4 GeV/c $\pi^-$ (KEK)
Overview of Achieved Detection Performances

Several MIMOSA chips (Strasbourg et al.) tested on H.E. beams (SPS, DESY) → well established perfo. :

- \( N \sim 10 \, e^- \leftrightarrow S/N \gtrsim 20 \rightarrow 30 \leftrightarrow \epsilon_{det} \gtrsim 99.5 \% \)
- \( \sigma_{sp} \sim 1.5 \, \mu m \)
- \( T_{oper.} \gtrsim 40 \, ^{\circ}C \)

- Best performing technology: AMS 0.35 \( \mu m \) OPTO (11–12 \( \mu m \) epitaxy; 20 \( \mu m \) option tests in Fall’06)
- Technology without epitaxy also shown to perform well: very high S/N but large clusters (hit separation \( \downarrow \))
- Macroscopic sensors: MIMOSA-5 (1.9 x 1.7 cm\(^2\); 1 Mpix), CAP-3 (0.3 x 2.1 cm\(^2\); 120 kpix)

- Thinning of MIMOSA-5 to 50 \( \mu m \) achieved → next : 35 \( \mu m \)
- Radiation tolerance \( \gtrsim 1 \, MRad, 10^{13} e^{\pm}_{10 \, MeV/cm^2}, 10^{12} n_{eq/cm^2} \leftrightarrow next : \gtrsim 10^{13} n_{eq/cm^2} \)
- Architecture with integrated discri. validated (\( \epsilon_{det} \gtrsim 99.3 \% ; \, fake \lesssim 10^{-3} \)) → next : integrated ADC & \( \varnothing \)
- Architecture with in-pixel memories & delayed r.o. well advanced (CAP/Hawaï, FAPS/RAL, MIMOSA/Strasbourg...)
MIMOSA sensors will equip STAR Heavy Flavour Tagger:

- 2008: analog output, 4 ms frame r.o. time
- 2011: digital output, $\lesssim 200 \mu s$ frame r.o. time

Similar sensors will equip EUDET (FP-6) beam telescope:

- 2007: demonstrator with analog output
- 2008: final device with digital output

CMOS sensors are also developed for:

- CBM Vertex Detector (FAIR/GSI $\gtrsim 2012$) $\rightarrow$ R&D on MIMOSA sensors for non-ion. rad. tol. (and speed)
- ILC Vertex Detector $\leftrightarrow$ R&D in France, UK, USA, Italy, ...
- BELLE Vertex Detector $\leftrightarrow$ R&D in Hawai

Spin-offs:

- Bio-medical imaging:
  - photo-electron detector (MIMOSA - Photonis) $\Omega$ H.E. electron microscope imager ; etc.
- Beam monitoring: MIMOTERA (SUCIMA / FP-5)
- Dosimetry
Application to the ILC Vertex Detector

- **Geometry:** 5 cylindrical layers (R=15 – 60 mm), $||\cos\theta|| \leq 0.90 – 0.96$

- $\sigma_{IP} = a \oplus b/p \cdot \sin^{3/2}\theta$, with $a < 5 \mu m$ and $b < 10 \mu m$ (SLD: $a = 8 \mu m$ and $b = 33 \mu m$)

- $t_{r.o.}$ (occupancy from beamstrahlung $e^{\pm}$):
  - $\approx 25 \mu s$ in L0
  - $\approx 50 \mu s$ in L1
  - $\approx 200 \mu s$ in L2, L3, L4

<table>
<thead>
<tr>
<th>Layer</th>
<th>Radius (mm)</th>
<th>Pitch (µm)</th>
<th>$t_{r.o.}$ (µs)</th>
<th>$N_{lad}$</th>
<th>$N_{pix}$ ($10^6$)</th>
<th>$P_{inst diss}$ (W)</th>
<th>$P_{mean diss}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L0</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>20</td>
<td>25</td>
<td>&lt;100</td>
<td>&lt;5</td>
</tr>
<tr>
<td>L1</td>
<td>25</td>
<td>25</td>
<td>50</td>
<td>26</td>
<td>65</td>
<td>&lt;130</td>
<td>&lt;7</td>
</tr>
<tr>
<td>L2</td>
<td>37</td>
<td>30</td>
<td>&lt;200</td>
<td>24</td>
<td>75</td>
<td>&lt;100</td>
<td>&lt;5</td>
</tr>
<tr>
<td>L3</td>
<td>48</td>
<td>35</td>
<td>&lt;200</td>
<td>32</td>
<td>70</td>
<td>&lt;110</td>
<td>&lt;6</td>
</tr>
<tr>
<td>L4</td>
<td>60</td>
<td>40</td>
<td>&lt;200</td>
<td>40</td>
<td>70</td>
<td>&lt;125</td>
<td>&lt;6</td>
</tr>
<tr>
<td>Total</td>
<td>142</td>
<td>305</td>
<td>&lt;565</td>
<td>&lt;29</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Ultra thin layers:** $\lesssim 0.2 \% X_0$/layer

- **Rad. tolerance (3 yrs):** $\lesssim 3 \cdot 10^{10} n_{eq}/cm^2$

- **Very low $P_{mean diss}$:** $<< 100$ W ($\rightarrow$ minimise cooling)

- **Rad. tolerance (3 yrs):** $\lesssim 6 \cdot 10^{12} e_{10MeV}/cm^2$ (150 kRad, $2 \cdot 10^{11} n_{eq}/cm^2$)
Mimosa 9: resolution vs pitch

Integration of CAP in (Super)BELLE
INTEGRATION OF SIGNAL PROCESSING FUNCTIONNALITIES
INSIDE PIXEL OR ON SENSOR PERIPHERY
MIMOSA-8: TSMC 0.25 $\mu$m digital fab. process ($\lesssim 7 \mu m$ epitaxy)
- 32 // columns of 128 pixels (pitch: 25 $\mu m$)
- 4 sub-arrays featuring AC and DC coupled on-pixel voltage amplif.
- on-pixel CDS
- discriminator at end of each column

Detection performance with 5 GeV/c e$^-$ beam (DESY):

![Graphs showing efficiency, average hit rate, and average hit multiplicity vs S/N cut for M8 digital.](image)

- Excellent m.i.p. detection performances despite modest thickness of epitaxial layer
  - det. eff. $\sim 99.3\%$ for fake rate of $\sim 0.1\%$
  - discriminated cluster multiplicity $\sim 3–4$

Archi. validated for next steps: techno. with thick epitaxy, rad. tol. pixel at $T_{room}$, ADC, $\varnothing$, etc.

19/05/06,
Fast col. // architecture (like MIMOSA-8), allowing to process signal (CDS, ADC, sparsification) during BX:
  ─ complex, close to technology limits ─ much design & test effort needed (but quite universal output)

Alternative ─ 2 phase \( \mu \)circuit architecture exploiting beam time structure, reducing data flux:
  1) charge stored (eventually sampled) inside pixel during train crossing: \( O(1) \) ms
  2) signal transferred and processed inbetween trains: \( O(100) \) ms

Different strategies of storage during train crossings:

\( 20 \sim 25 \, \mu m \) large pixels with \( \geq 20 \) capacitors
  \( \leq 50 \, \mu s \) long snapshots/capacitor
\( \lesssim 5 \, \mu m \) large pixels with 1 capa.(hit position)
  and \( 50 \, \mu m \) large pixels for hit zone selection

Difficulty: are small capacitors precise enough?
Difficulty: can cluster size be \( \lesssim 3 \) pixels?
Constraints on Integrated ADC

- Ensure $\epsilon_{\text{det}} > 99\%$ with very few fake hits, $\sigma_{IP} \sim$ few $\mu m$ & double hit separation

$\Rightarrow$ distinguish small Q deposits due to: $\star$ negative Landau fluctuations (seed) $\star$ pixels in cluster crown

$\nabla \nabla \nabla \nabla \geq 3$ effective bits OK $\Rightarrow$ base line: 4 – 5 bits $\Rightarrow$ epitaxy thickness of final prod. techno. ????

- Read-out frequency: $\geq 10 \text{ MHz} / \text{column}$ or $\geq 20 \text{ MHz} / \text{pair of columns}$

- Dimensions: $20$–$30 \times 1000 \mu m^2 / \text{column}$

or $40$–$60 \times 1000 \mu m^2 / \text{pair of columns}$

- Power consumption: $\lesssim 0.5 \text{ mW} / \text{column}$ or $1 \text{ mW} / \text{pair of columns}$

$\Leftarrow$ Optimised ADC architecture is still to be found out: flash, semi-flash, succ. approx., Wilkinson, ...
Improving Charge Collection & Signal Proc. Capabilities

► Increase collected charge by enlarging depleted volume:

- increasing N-well potential (very limited possibilities)
- enlarging surface of N-wells inside pixels (increase capacitance noise)

► Ex: triple-well technology (STM 0.13 $\mu m$)

(see L.Ratti):

- Buried n-channel electrode:
  - Try integrating signal processing $\mu$circuits
  - self triggered pixels (?
- Test structures under study

► Ex: unidepleted active pixel sensors

( see P.Rehak):

- Pixels composed of concentric rings of n-wells:
  - Can they host P-MOS T for signal processing?
RADIATION TOLERANCE
Neutrons of O(1 MeV) at JINR (Dubna):
  irradiation with up to $10^{13} n_{eq}/cm^2$

Tests with 2 sensors ($T = +10^\circ C$)
from different fabrication processes:
  - AMS-0.6 ($\lesssim 14 \mu m$ epitaxy)
  - AMI-0.35 ($\sim 4 \mu m$ epitaxy)
    $\longrightarrow$ charge loss for $\lesssim 10^{12} n_{eq}/cm^2$
    & modest increase of $I_{leak}$ & noise ($\lesssim 10\%$)

AMS-0.35 OPTO ($\sim 11 \mu m$ epitaxy) $\triangleright$ S/N (MPV) vs fluence and T (tests at CERN-SPS):

<table>
<thead>
<tr>
<th>Fluence</th>
<th>$T = -20^\circ C$</th>
<th>$T = 0^\circ C$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>28.4 ± 0.2</td>
<td>26.3 ± 0.2</td>
</tr>
<tr>
<td>$10^{11} n_{eq}/cm^2$</td>
<td>25.3 ± 0.2</td>
<td>24.5 ± 0.4</td>
</tr>
<tr>
<td>$3\cdot10^{11} n_{eq}/cm^2$</td>
<td>—</td>
<td>23.0 ± 0.2</td>
</tr>
<tr>
<td>$10^{12} n_{eq}/cm^2$</td>
<td>18.7 ± 0.2</td>
<td>—</td>
</tr>
</tbody>
</table>

Conclusion: fluences of $\gtrsim 10^{12} n_{eq}/cm^2$ affordable
  (better performances with $T < 0^\circ C$)
  $\rightarrow \epsilon_{det} \sim 99.74 \pm 0.08\%$ ($10^{12} n_{eq}/cm^2; T = -20^\circ C$)

$\triangleright \triangleright$ Results show that fluences $\gtrsim 1\cdot10^{13} n_{eq}/cm^2$ can presumably be accommodated
Means to Improve Tolerance to Non-Ionising Radiation

- Reduce mean free path of signal $e^{-}$:
  - Reduce pixel pitch (optimise w.r.t. r.o. speed)
  - Improve efficiency of charge collection system (pixel design optimisation)
  - Optimise operation temperature
  - Investigate annealing possibilities

- Improve S/N performance:
  - Optimise pixel and r.o. architecture
  - Investigate thick epitaxy techno. $\leftrightarrow$ AMS 0.35 OPTO ”20 $\mu m$” epitaxy option
  - Optimise cluster reconstruction algorithms

- Equip each detector layer with 2 layers of sensors
  $\leftrightarrow$ 90 % detection efficiency per layer allows 99 % overall detection efficiency
  - double layer $\leftrightarrow$ track mini-segments from loosely selected clusters $\leftrightarrow$ improved detection efficiency
  - Thinning sensors to ultimate thickness ($\sim 35 \mu m$) is particularly valuable
  - Design mechanical support allowing double sensor layer per detector layer
3 major effects expected from ionising radiation:

- Shift of threshold voltages: $\propto$ Nb(holes) created & trapped in gate oxide $\propto$ oxide thickness
  $\rightarrow$ aim for $\lesssim 10$ nm thick oxide ($\sim$ the case for $\leq 0.35 \mu m$ technologies)

- Leakage current in NMOS transistors

- Leakage current in N-channel intertransistors

Aim for short integration time and for $T \lesssim 0^\circ C$
Modified pixel design:
- removal of thick oxide nearby the N-well (against charge accumulation)
- implantation of P+ guard-ring in polysilicon around N-well (against leakage current)

Beamtest on MIMOSA11

Running conditions: +40°C, 700µs readout time

<table>
<thead>
<tr>
<th></th>
<th>New</th>
<th>After 20kRad</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard pixel (A0 Sub 2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S/N (MPV)</td>
<td>23.9</td>
<td>10.3</td>
</tr>
<tr>
<td>Det Eff [%]</td>
<td>99.9</td>
<td>97.7</td>
</tr>
<tr>
<td>Noise [e⁻]</td>
<td>10.7</td>
<td>23.5</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>New</th>
<th>After 20kRad</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardened pixel (A0 Sub 1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S/N (MPV)</td>
<td>14.9</td>
<td>15.1</td>
</tr>
<tr>
<td>Det Eff [%]</td>
<td>99.5</td>
<td>99.6</td>
</tr>
<tr>
<td>Noise [e⁻]</td>
<td>16.1</td>
<td>16.1</td>
</tr>
</tbody>
</table>
Noise performance of pixel adapted to ionising radiation: Noise ($e^-$ ENC) vs Integration time (ms) for Ordinary and Radiation Tolerant pixels, measured at $T = -25^\circ C, +10^\circ C$ and $+40^\circ C$.

**-25 °C**

**10 °C**

**40 °C**

1 MRad tolerance demonstrated (esp. at $T < 0^\circ C$) Room for improvement

19/05/06,
Comparison of charge collection efficiency after 10 keV X-Ray irradiation for 2 different technologies

MIMOSA prototypes manufactured in AMI-0.35 and AMS-0.35 OPTO
and tested with $^{55}$Fe at $T = +10^\circ$C before/after irradiation:

- AMI-0.35 : 400 kRad, 3.3 ms integration time
- AMS-0.35 OPTO : 1 MRad, 0.7 ms integration time

AMS-0.35 OPTO sensor does not exhibit any observable drop in charge coll. efficiency after 1 MRad
Charge loss consecutive to ionising radiation seems related to positive oxide charge build-up at Si-SiO$_2$ interfaces ⇒ relatively strong potential depleting P+ coating of N-MOS T

part of the signal electrons get attracted and do not reach the charge collecting diode

The effect seems technology dependent ⇒ different P+ coating of N-MOS T (?)

not predictable (fabrication parameter)

Gain: 6.4 e/ADC
LCurrent: 3.6 fA ⇒ 31 fA
Noise: 17 e ⇒ 21 e

$I_{irr}/I_0 = 8.6$
$N_{irr}/N_0 = 1.2$
SUMMARY
### SUMMARY

- **CMOS sensor technology R&D started in 1999:**
  - now assessed quite extensively → attractive tracking/vertexing performances well established
  - ~ ready to equip high precision tracking detectors (provided rad. levels and r.o. speed are not “extreme”)
  - 1st detector made of CMOS sensors should be commissioned in a few years:
    - STAR-HFT: 1) 2008, 2) 2011
    - BELLE-VD (~ 2010 ?)
    - EUDET beam telescope: 1) 2007, 2) 2008

- Wide spectrum of CMOS sensor potential still poorly explored/exploited (e.g. integrated signal processing):
  - Strong, growing, R&D community able to undertake the challenge:
    - ~ 10 groups involved in chip design
    - > 10 groups concentrating on tests and integration issues
    - several issues poorly covered → newcomers ...
  - Several demanding mid-term applications under way:
    - ILC (~ 2015)
    - CBM (> 2012)
    - etc.
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Main R&D efforts in the coming years:

- Fast col. // architecture with integ. ADC & sparsification
- Charge collection systems with improved S/N
- Complete thinning ~ 50 $\mu m$ & try < 35 $\mu m$
- Trade-off: $P_{\text{diss.}} / T_{\text{oper.}} / \text{cooling} / \text{mat.bud.}, \ldots$

▶▶▶ Right time to combine & share knowledge & efforts (?)
- several spin-offs in imaging

19/05/06,