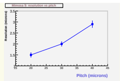
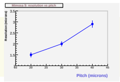


Adapting CMOS Sensors to Future Vertex Detectors

Marc Winter (IReS/IPHC-Strasbourg)

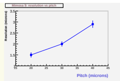
OUTLINE

- **Remarks on experimental trends ⟼ Limits of existing devices for flavour tagging**
- **The solution of CMOS sensors:**
  ↪ Principle of operation – Advantages & Concerns – R&D directions – Typical performances
- **Tracking detector applications foreseen: decided or ambitionned**
- **Current R&D frontier : signal processing architectures – radiation tolerance**
- **Summary**



WHAT IS DRIVING THE R&D

ON CMOS SENSORS ?



General Trend in Vertexing Requirements (1/2)

■ **Flavour tagging takes growing importance in understanding the dynamics underlying**

heavy ion and particle physics phenomena ⟼ b, c, τ tagging with High Efficiency & Purity !

▶ **Ex: ILC physics programme ⟼ high performance flavour identification is a MUST for most events :**

- **b, c, τ contained in most final states:**

$$\mathbf{t} \longrightarrow \mathbf{Wb} \,;\; \mathbf{W} \longrightarrow \mathbf{c\bar{s}} \,;\; \mathbf{Z} \longrightarrow \mathbf{b\bar{b}}, \mathbf{c\bar{c}}, \tau\bar{\tau} \,; \qquad \chi^{\pm} \longrightarrow \mathbf{W}^{\pm}\chi^{\mathbf{0}} \,;\; \chi^{\mathbf{0}}_{\mathbf{2}} \longrightarrow \mathbf{Z}\chi^{\mathbf{0}}_{\mathbf{1}};$$

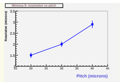
↪ **use b, c, τ decays of Z and W bosons to enhance sensitivity to new physics:**

▷ **background rejection – measurements of $\mathbf{Br(H,X)}$, $\mathbf{A_{FB}}$, $\mathbf{A_{LR}}$, etc.**

- **assign EACH track to its vertex origin (1^{ry}, 2^{ry}, 3^{ry}) in a POLY-JET environnement (Q$_{\mathbf{Vx}}$, E$_{\mathbf{flow}}$!)**

  and establish links between 2^{ry} and 3^{ry} vertices ⟶ reconstruct decay chains:

$$\mathbf{e^+e^-} \longrightarrow \mathbf{t\bar{t}} \longrightarrow \mathbf{b\bar{b}WW} \longrightarrow \;\geq \text{6 jets}$$
$$\mathbf{e^+e^-} \longrightarrow \mathbf{t\bar{t}H} \longrightarrow \mathbf{b\bar{b}b\bar{b}WW} \longrightarrow \;\geq \text{8 jets}$$
$$\mathbf{e^+e^-} \longrightarrow \mathbf{HA} \longrightarrow \mathbf{t\bar{t}t\bar{t}} \longrightarrow \mathbf{b\bar{b}b\bar{b}WWWW} \longrightarrow \;\geq \text{12 jets}$$



General Trend in Vertexing Requirements (2/2)

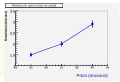
▷▷▷ Aim for an ultra-light, very granular, poly-layer Vertex Detector installed very close to the interaction point

▷▷▷ Demanding running conditions (occupancy, radiation) !!!

▷▷▷ **Existing technologies are not adequate:**

- ⋇ CCD (SLD): granular and thin BUT too slow and radiation soft
- ⋇ Hybrid Pixel Sensors (Tevatron, LHC): fast and radiation hard BUT not granular and thin enough

▷▷▷ **CMOS sensors** are expected to provide an attractive trade-off between granularity, material budget, radiation tolerance and speed



PRINCIPLE OF OPERATION

AND SPECIFIC FEATURES

OF CMOS SENSORS

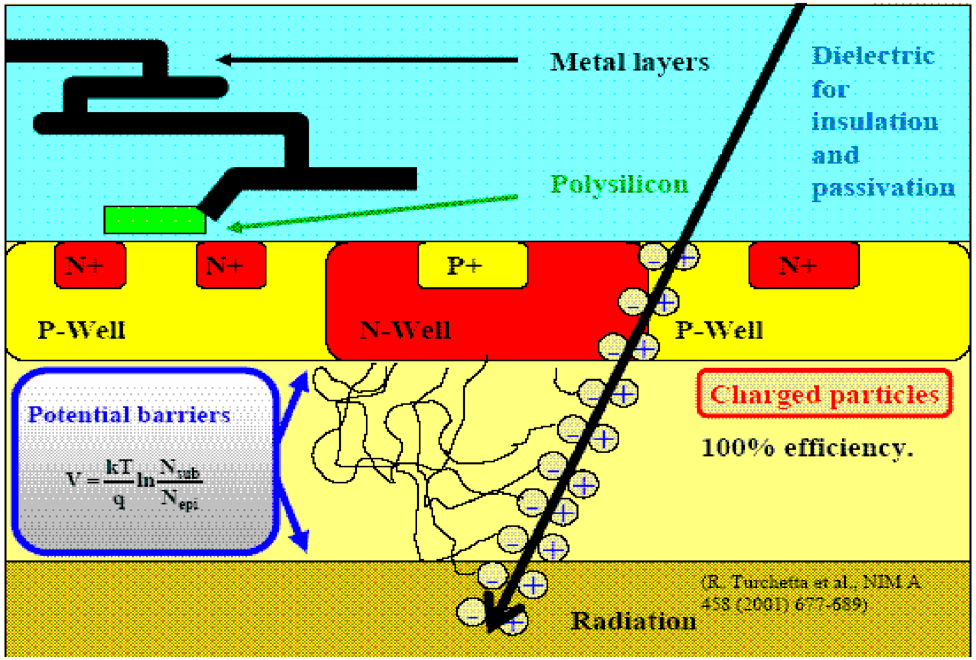
Main Features and Advantages of CMOS Sensors

- **p-type low-resistivity Si hosting n-type ”charge collectors”**
  - signal created in epitaxial layer (low doping):

    Q $\sim$ 80 e-h / μm $\mapsto$ signal $\lesssim$ 1000 e^{-}
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode

    with help of reflection on boundaries

    with p-well and substrate (high doping)

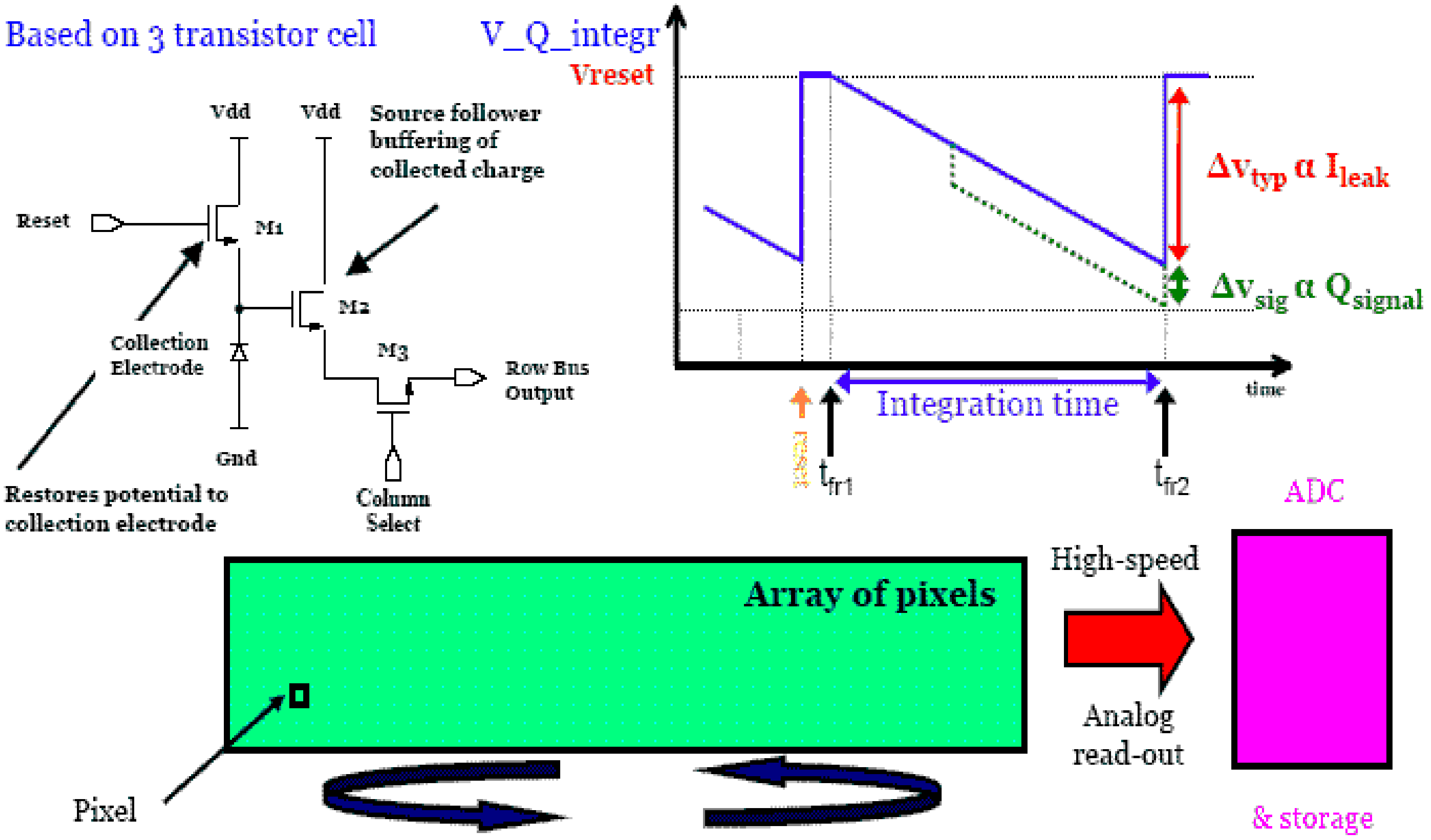


(R. Turchetta et al., NIM A 458 (2001) 677-689)

- **Specific advantages of CMOS sensors:**
  - ◇ Signal processing μcircuits integrated on sensor substrate (system-on-chip) $\mapsto$ compact, flexible
  - ◇ Sensitive volume ($\sim$ epitaxial layer) is $\sim$ 10–15 μm thick $\longrightarrow$ thinning to $\lesssim$ 30 μm permitted
  - ◇ Standard, massive production, fabrication technology $\longrightarrow$ cheap, fast turn-over
  - ◇ As granular and thin as CCDs, BUT faster and more radiation tolerant

Basic Read-Out Architecture

Based on 3 transistor cell

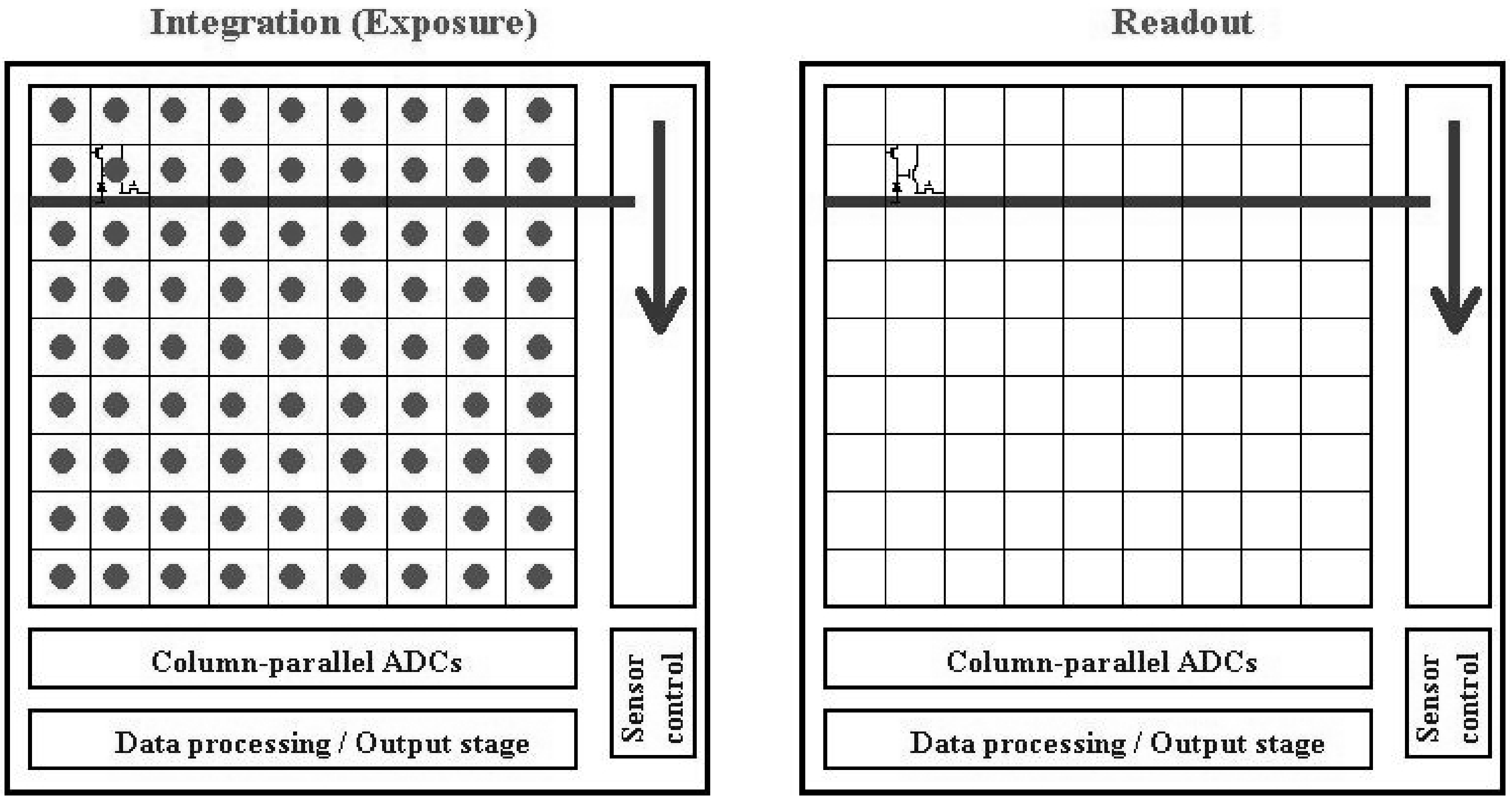


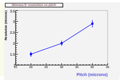
Pixel Array: Column select – ganged row read

Low power – only significant draw at readout edge

Basic Read-Out Architectures

- **Two different ways of reading out the sensor:**
  - ◇ Rolling Shutter mode (see below): array is read out row after row
    - ↪ each row is slightly shifted in time w.r.t. previous ones
  - ◇ Snap-shot mode (rather suited to imaging): all rows read out at once
    - ↪ dead time before/during pulsing all rows and during read-out





Main R&D Directions

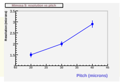
- **High r.-o. speed, low noise, low power dissip., highly integrated signal processing architecture:**
  - analog part (charge collection, pre-amp, CDS, ...) inside pixel
  - mixed (ADC) and digital (sparsification) micro-circuits integrated inside pixel or aside of active surface

- **Optimal fabrication process:**
  - epitaxial layer thickness
  - number of metal layers
  - yield
  - (dark current)
  - cost
  - life time of process

- **Radiation Tolerance:**
  - dark current
  - doping profile
  - (latch-up)

- **Room temperature operation:**
  - minimise cooling requirements
  - performances after irradiation

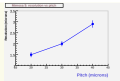
- **Industrial thinning procedure:**
  - minimal thickness
  - individual chips rather than wafers
  - yield



M.I.P. TRACKING PERFORMANCES:

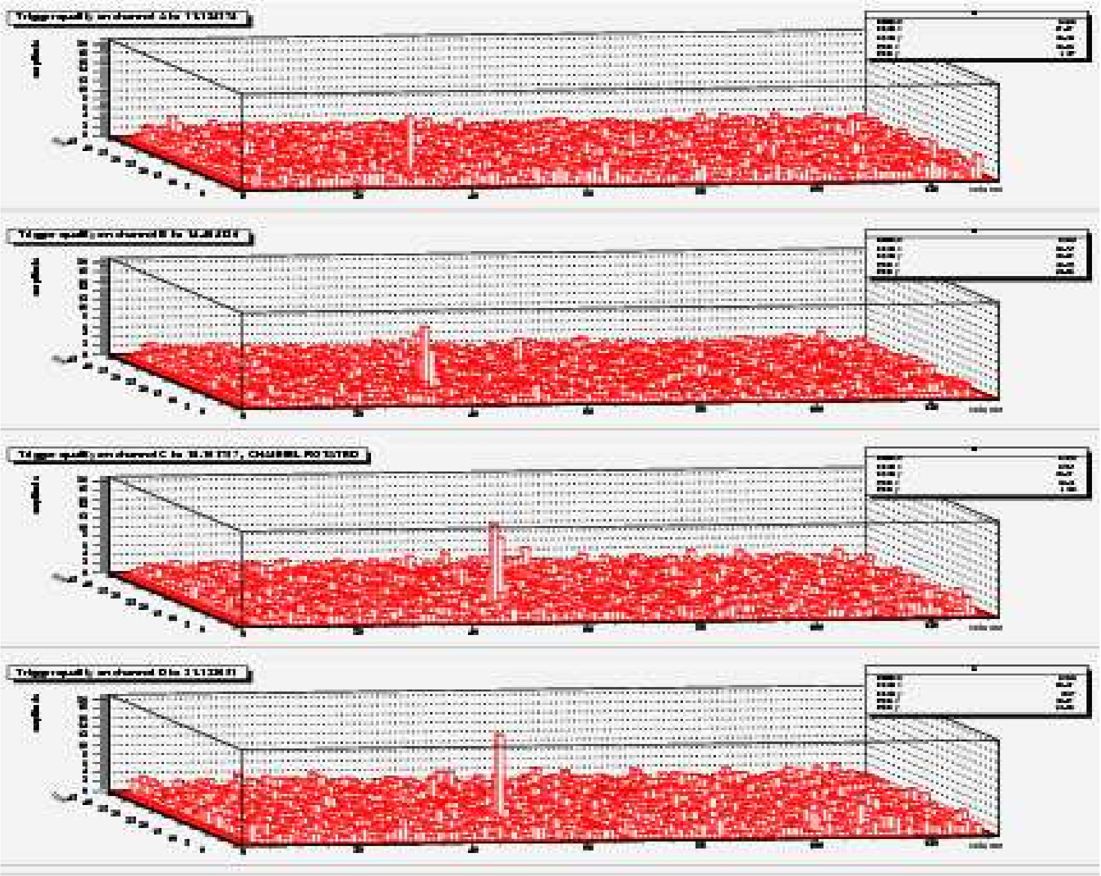
PIXEL & CLUSTER CHARACTERISTICS,

DETECTION EFFICIENCY



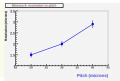
CMOS Sensor ”Community”

- **Several groups design CMOS sensors for charged particle tracking :**
  - **BELLE upgrade ↦ SuperBELLE:**
    Univ.Hawaï
  - **STAR upgrades:**
    IReS/IPHC (Strasbourg)
  - **ILC (EUDET ⊂ E.U. FP-6):**
    IReS/IPHC (Strasbourg), DAPNIA (Saclay),
    LPC (Clermont), LPSC (Grenoble),
    Univ.Roma-3, Univ.Bergamo, Univ. Pisa,
    RAL, LBL, BNL, Univ.Oregon & Yale (SARNOF**)**
    others (?)
  - **CBM (GSI):**
    IReS/IPHC (Strasbourg)



R&D for Super BELLE: **hits in 1st beam telescope made of 4 CAP-2 sensors exposed to 4 GeV/c π^- (KEK)**

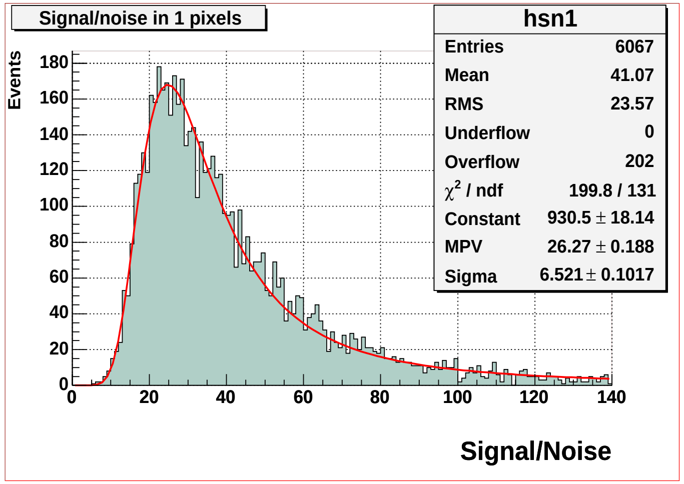
- **Several other groups involved in chip characterisation & detector integration issues**

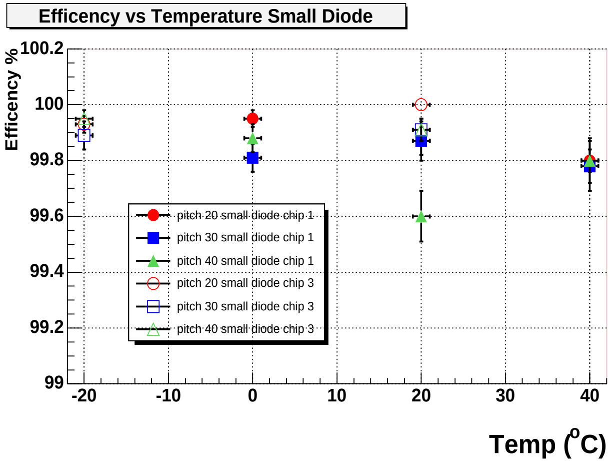


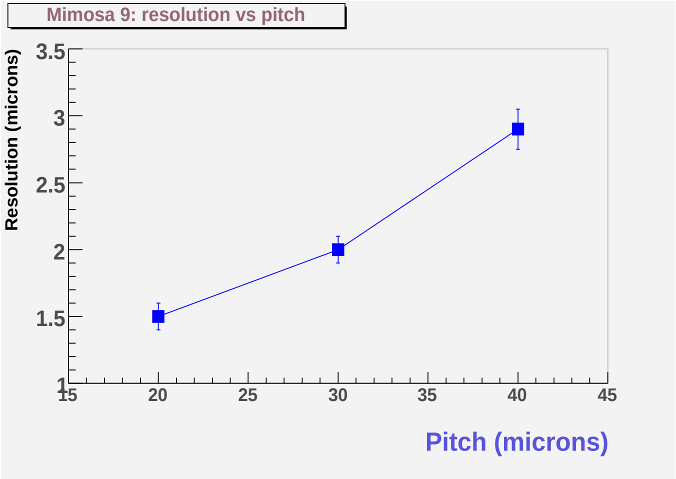
Overview of Achieved Detection Performances

Several MIMOSA chips (Strasbourg et al.) tested on H.E. beams (SPS, DESY) $\mapsto$ well established perfo. :

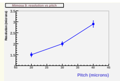
- N $\sim$ 10 e$^-$ $\mapsto$ S/N $\gtrsim$ 20 – 30 $\mapsto$ ϵ_{det} $\gtrsim$ 99.5 % ● σ_{sp} $\sim$ 1.5 μm ● $T_{oper.}$ $\gtrsim$ 40 °C
- Best performing technology: AMS 0.35 μm OPTO (11–12 μm epitaxy; 20 μm option tests in Fall'06)
- Technology without epitaxy also shown to perform well: very high S/N but large clusters (hit separation $\searrow$)
- Macroscopic sensors : MIMOSA-5 (1.9 x 1.7cm^2; 1 Mpix), CAP-3 (0.3 x 2.1cm^2; 120 kpix)







- Thinning of MIMOSA-5 to 50 μm achieved $\mapsto$ next : 35 μm
- Radiation tolerance $\gtrsim$ 1 MRad, $10^{13} e^{\pm}_{10\ MeV}$/cm^2, 10^{12}n$_{eq}$/cm^2 $\mapsto$ next : $\gtrsim$ 10^{13}n$_{eq}$/cm^2
- Architecture with integrated discri. validated (ϵ_{det} $\gtrsim$ 99.3 % ; fake $\lesssim$ 10^{-3}) $\mapsto$ next : integrated ADC & $\emptyset$
- Architecture with in-pixel memories & delayed r.o. well advanced (CAP/Hawaï, FAPS/RAL, MIMOSA/Strasbourg...)



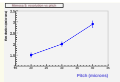
Established and Potential Applications CMOS Sensors

- **MIMOSA sensors will equip STAR Heavy Flavour Tagger:**
  - **2008: analog output, 4 ms frame r.o. time**
  - **2011: digital output, $\lesssim$ 200 μs frame r.o. time**

▷ **similar sensors will equip EUDET (FP-6) beam telescope:**
  - **2007: demonstrator with analog output**
  - **2008: final device with digital output**

- **CMOS sensors are also developed for:**
  - **CBM Vertex Detector (FAIR/GSI $\gtrsim$ 2012) $\longmapsto$ R&D on MIMOSA sensors for non-ion. rad. tol. (and speed)**
  - **ILC Vertex Detector $\longmapsto$ R&D in France, UK, USA, Italy, ...**
  - **BELLE Vertex Detector $\longmapsto$ R&D in Hawaï**

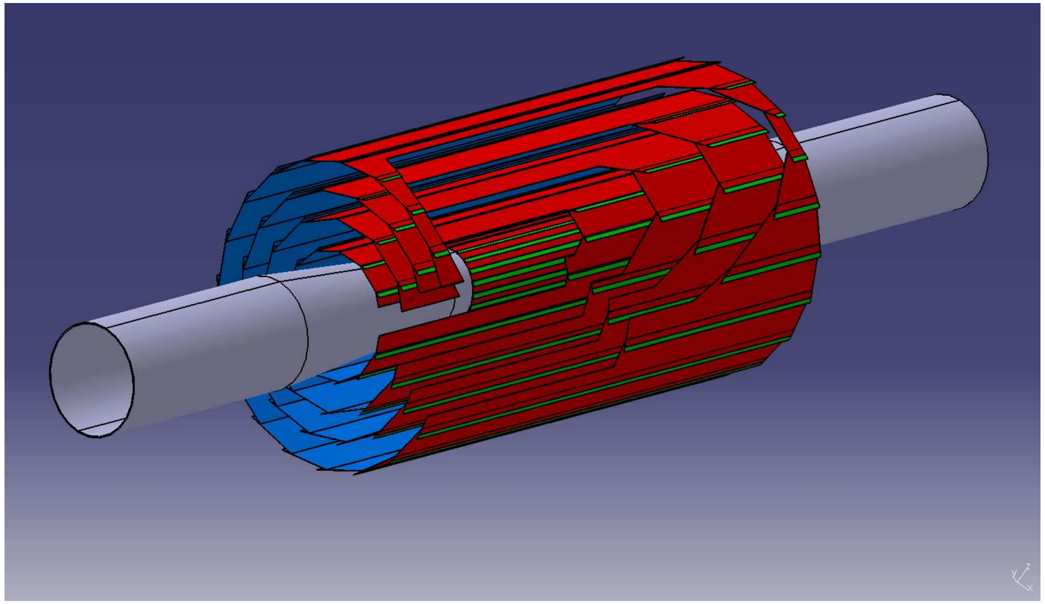
- **Spin-offs :**
  - **Bio-medical imaging :**
    - **photo-electron detector (MIMOSA - Photonis)**
    - **H.E. electron microscope imager ; etc.**
  - **Beam monitoring : MIMOTERA (SUCIMA / FP-5)**
  - **Dosimetry**



Application to the ILC Vertex Detector

- **Geometry: 5 cylindrical layers (R=15 – 60 mm), $||cos\theta|| \leq$ 0.90 – 0.96**
- $\mathbf{\sigma_{IP} = a \oplus b/p \cdot sin^{3/2}\theta}$, **with a $<$ 5 μm and b $<$ 10 μm (SLD: a = 8 μm and b = 33 μm)**
- **$t_{r.o.}$ (occupancy from beamstrahlung $e^{\pm}$): ¶ 25 μs in L0 ¶ 50 μs in L1 $\Bumpeq$ $\lesssim$ 200 μs in L2, L3, L4**

Layer	Radius (mm)	Pitch (μm)	$t_{r.o.}$ (μs)	N_{lad}	N_{pix} (10^6)	P_{diss}^{inst} (W)	P_{diss}^{mean} (W)
L0	**15**	20	25	20	25	$<$100	$<$**5**
L1	**25**	25	50	26	65	$<$130	$<$**7**
L2	**37**	30	$<$200	24	75	$<$100	$<$**5**
L3	**48**	35	$<$200	32	70	$<$110	$<$**6**
L4	**60**	40	$<$200	40	70	$<$125	$<$**6**
Total				142	**305**	$<$565	$<$**29**

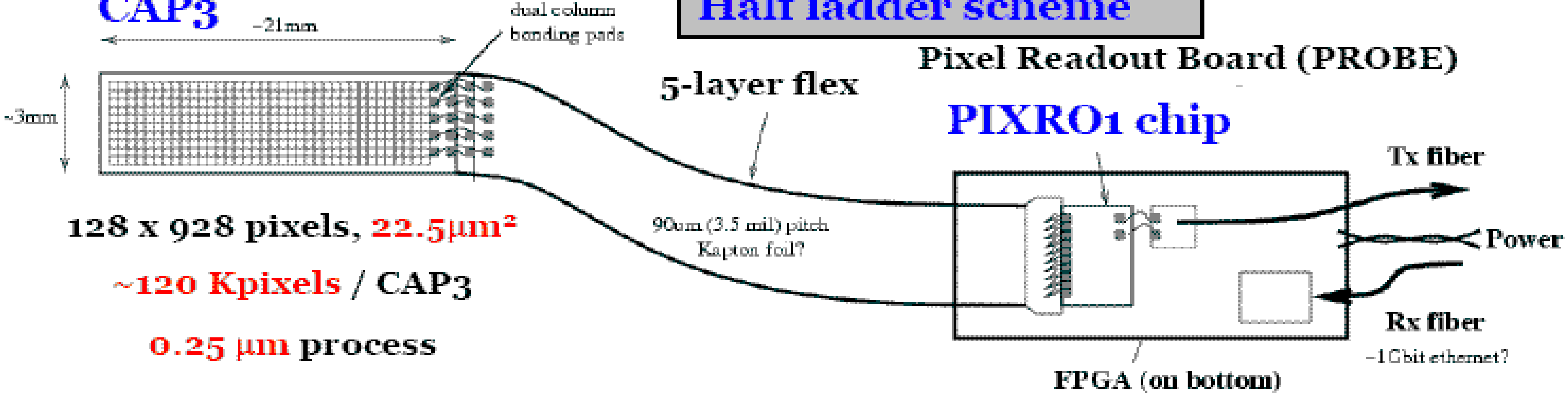


- **Ultra thin layers: $\lesssim$ 0.2 % X_0/layer**
- **Very low P_{diss}^{mean}: $<<$ 100 W ($\mapsto$ minimise cooling)**
- **Rad. tolerance (3 yrs): $\lesssim$ 3·10^{10} n_{eq}/cm^2 – $\lesssim$ 6·10^{12} e_{10MeV}/cm^2 (150 kRad, 2·10^{11} n_{eq}/cm^2)**

Integration of CAP in (Super)BELLE

CAP3

Half ladder scheme

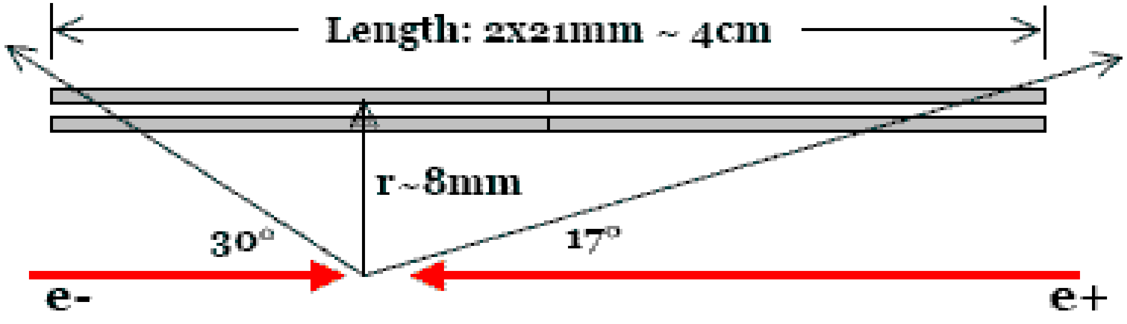


128 x 928 pixels, 22.5µm²

~120 Kpixels / CAP3

0.25 µm process

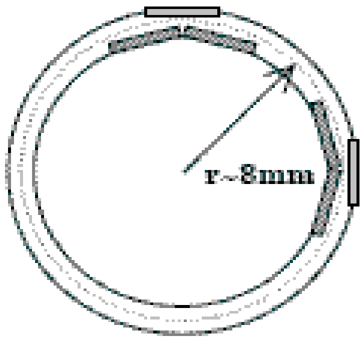
Side view

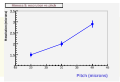


# of Detector / layer ~ 32

End view

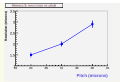
Double layer, offset structure



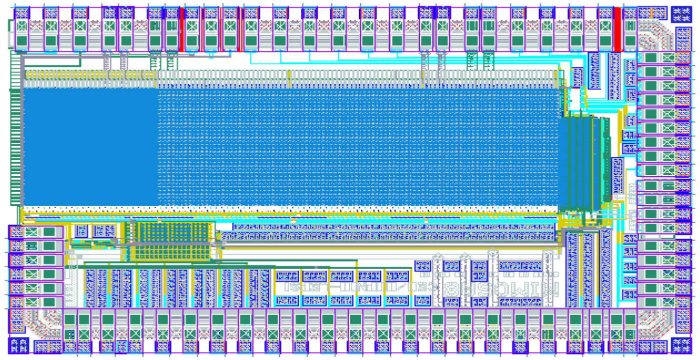


INTEGRATION OF SIGNAL PROCESSING FUNCTIONNALITIES

INSIDE PIXEL OR ON SENSOR PERIPHERY

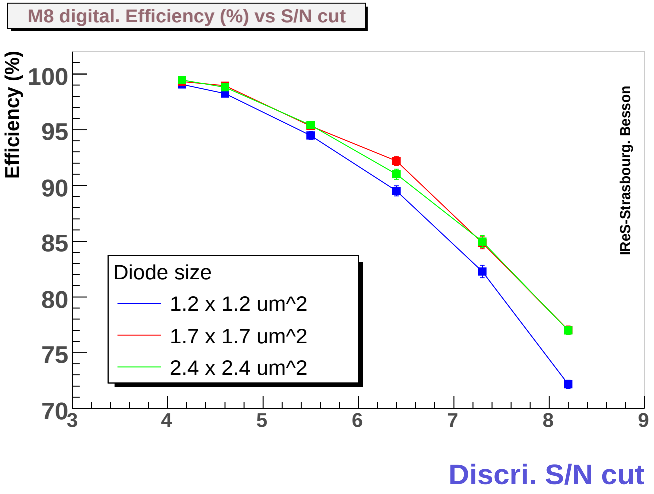


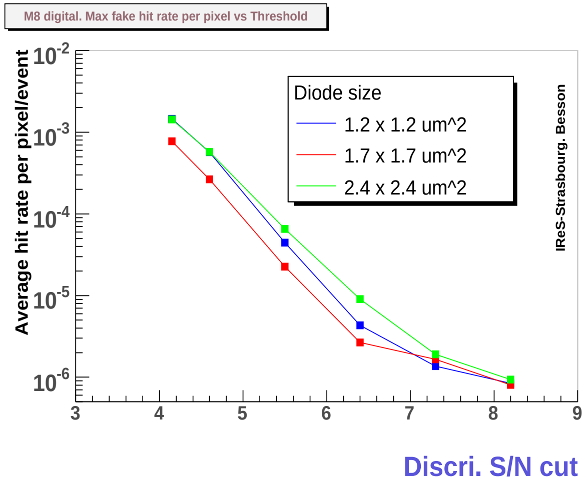
High Read-Out Speed Architecture

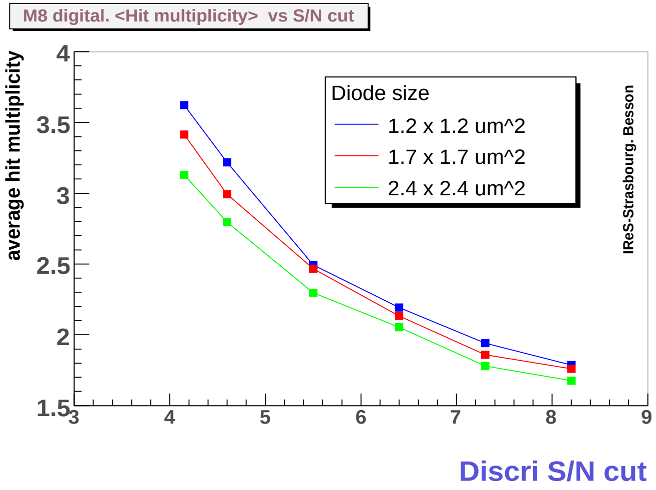


- **MIMOSA-8: TSMC 0.25 μm digital fab. process ($\lesssim$ 7 μm epitaxy)**
  - **32 // columns of 128 pixels (pitch: 25 μm)**
  - **4 sub-arrays featuring AC and DC coupled on-pixel voltage amplif.**
  - **on-pixel CDS**
  - **discriminator at end of each column**

- **Detection performance with 5 GeV/c e$^-$ beam (DESY):**



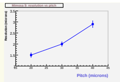




▷▷ **Excellent m.i.p. detection performances despite modest thickness of epitaxial layer**

◇ **det. eff. $\sim$ 99.3 % for fake rate of $\sim$ 0.1 %** ◇ **discriminated cluster multiplicity $\sim$ 3–4**

▷▷ **Archi. validated for next steps: techno. with thick epitaxy, rad. tol. pixel at T$_{room}$, ADC, $\varnothing$, etc.**



Application to ILC: Various FE Architectures

▷ **Fast col. // architecture (like MIMOSA-8), allowing to process signal (CDS, ADC, sparsification) during BX:**

$\hookrightarrow$ complex, close to technology limits $\mapsto$ much design & test effort needed (but quite universal output)

▶ **Alternative $\mapsto$ 2 phase μcircuit architecture exploiting beam time structure, reducing data flux:**

1) charge stored (eventually sampled) inside pixel during train crossing: O(1) ms

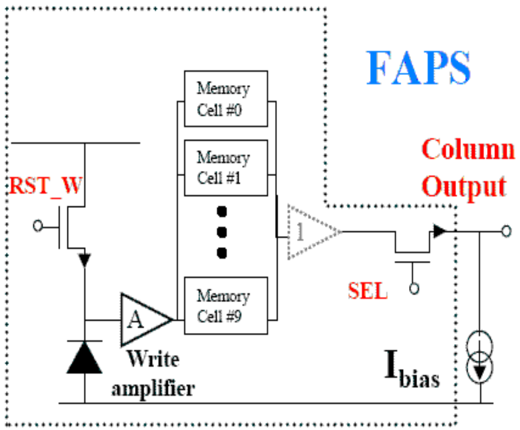
2) signal transfered and processed inbetween trains: O(100) ms

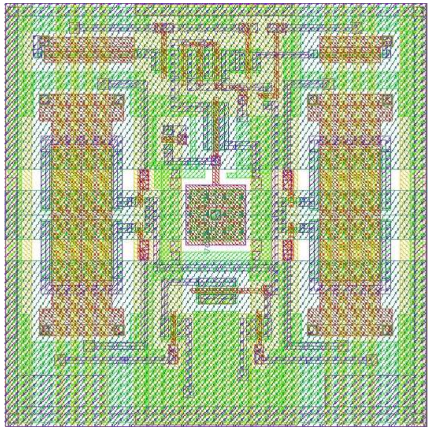
▶ **Different strategies of storage during train crossings:**

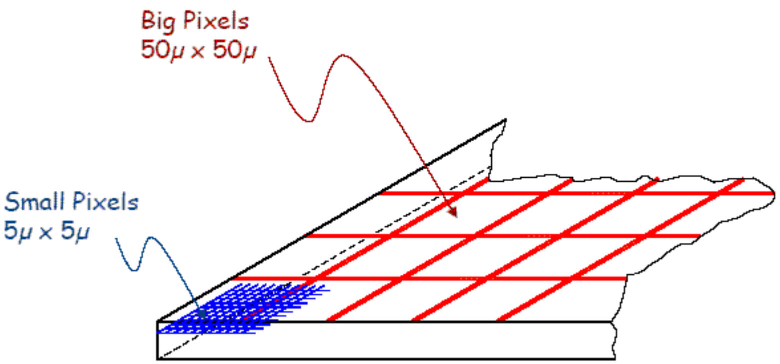
$\therefore$ 20 – 25 μm large pixels with $\gtrsim$ 20 capacitors

$\hookrightarrow$ $\lesssim$ 50 μs long snapshots/capacitor

$\therefore$ $\lesssim$ 5 μm large pixels with 1 capa.(hit position) and 50 μm large pixels for hit zone selection

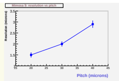






▷ **Difficulty:** are small capacitors precise enough ?

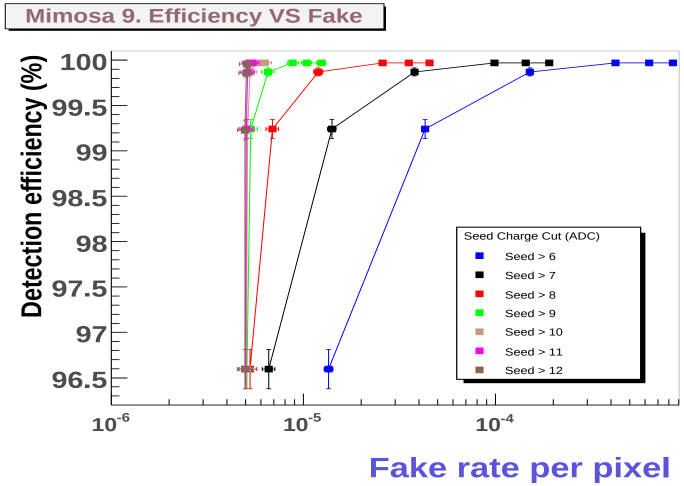
▷ **Difficulty:** can cluster size be $\lesssim$ 3 pixels ?

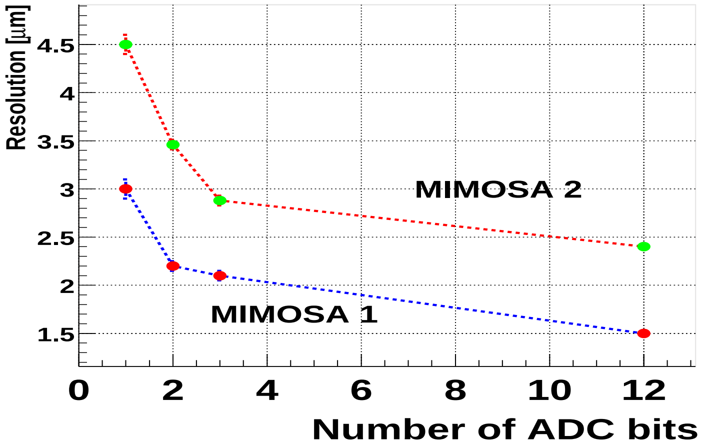


Constraints on Integrated ADC

- Ensure $\epsilon_{\mathrm{det}} > 99$ % with very few fake hits, $\sigma_{\mathrm{IP}} \sim$ few μm & double hit separation

$\Rrightarrow$ distinguish small Q deposits due to: ⋇ negative Landau fluctuations (seed) ⋇ pixels in cluster crown

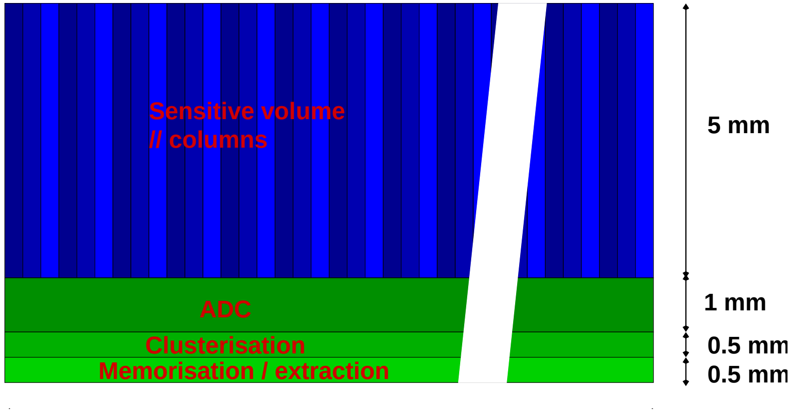




▷▷▷ $\geq$ 3 effective bits OK $\mapsto$ base line: 4 – 5 bits $\rightarrowtail$ epitaxy thickness of final prod. techno. ????

- Read-out frequency : $\geq$ 10 MHz / column or $\geq$ 20 MHz / pair of columns
- Dimensions : 20–30 x 1000 μm^2 / column

  or 40–60 x 1000 μm^2 / pair of columns
- Power consumption : $\lesssim$ 0.5 mW / column or 1 mW / pair of columns



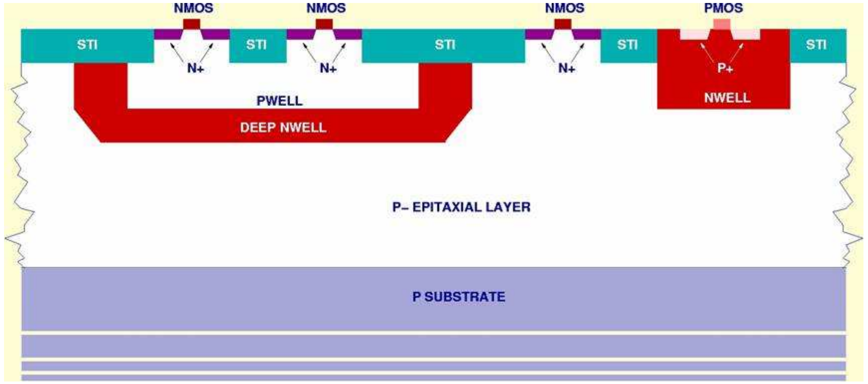
$\hookrightarrow$ Optimised ADC architecture is still to be found out: flash, semi-flash, succ. approx., Wilkinson, ...

Improving Charge Collection & Signal Proc. Capabilities

▶ **Increase collected charge by enlarging depleted volume:**

- **increasing N-well potential (very limited possibilities)**
- **enlarging surface of N-wells inside pixels ($\longmapsto$ increases capacitance noise)**
  - $\hookrightarrow$ **use N-well to integrate P-MOS T for signal processing**

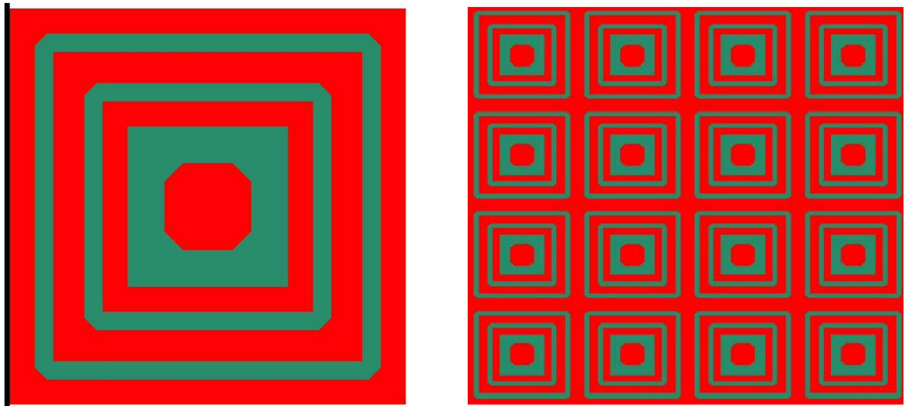
▶ **Ex: triple-well technology (STM 0.13 μm)**
(see L.Ratti) :



▷ **Buried n-channel electrode:**

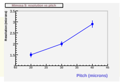
- ◇ **Try integrating signal processing μcircuits**
  - $\hookrightarrow$ **self triggered pixels (?)**
- ◇ **Test structures under study**

▶ **Ex: unidepleted active pixel sensors**
(see P.Rehak) :

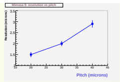


▷ **Pixels composed of concentric rings of n-wells:**

- ◇ **Can they host P-MOS T for signal processing ?**



RADIATION TOLERANCE



Radiation Tolerance: Non-Ionising Radiation

- **Neutrons of O(1 MeV) at JINR (Dubna):**

  irradiation with up to $10^{13} n_{eq}/cm^2$

- **Tests with 2 sensors (T = + 10°C)**

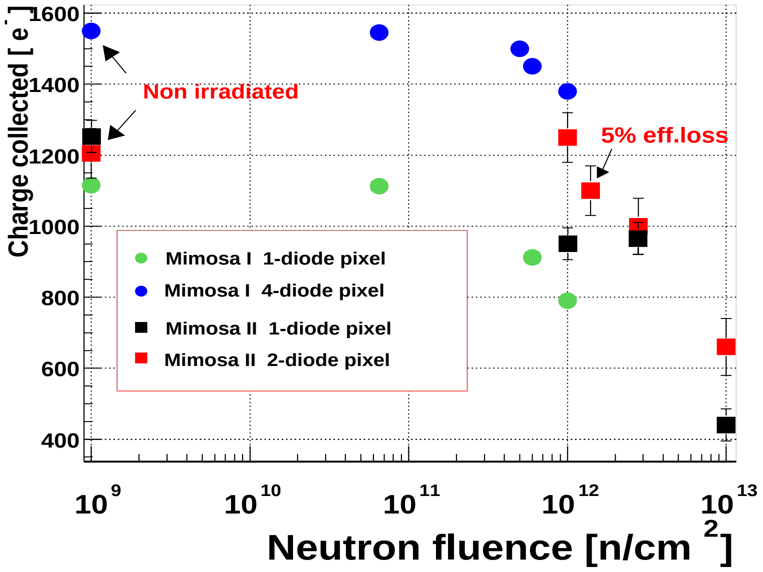
  from different fabrication processes:

  ◇ AMS-0.6 ($\lesssim$ 14 μm epitaxy)

  ◇ AMI-0.35 ($\sim$ 4 μm epitaxy)

  $\hookrightarrow$ charge loss for $\lesssim 10^{12} n_{eq}/cm^2$

  & modest increase of I_{leak} & noise ($\lesssim$ 10 %)



- **AMS-0.35 OPTO ($\sim$ 11 μm epitaxy) $\triangleright$ S/N (MPV) vs fluence and T (tests at CERN-SPS):**

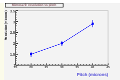
Fluence	T = -20°C	T = 0°C
0	28.4 $\pm$ 0.2	26.3 $\pm$ 0.2
10^{11} n_{eq}/cm^2	25.3 $\pm$ 0.2	24.5 $\pm$ 0.4
$3 \cdot 10^{11}$ n_{eq}/cm^2	—	23.0 $\pm$ 0.2
10^{12} n_{eq}/cm^2	**18.7 $\pm$ 0.2**	—

Conclusion: fluences of $\gtrsim 10^{12} n_{eq}/cm^2$ affordable

(better performances with T $<$ 0°C)

$\rightarrowtail$ $\epsilon_{det} \sim$ 99.74 $\pm$ 0.08 % ($10^{12} n_{eq}/cm^2$; T = -20°C)

$\triangleright\triangleright$ **Results show that fluences $\gtrsim 1 \cdot 10^{13} n_{eq}/cm^2$ can presumably be accomodated**



- Means to Improve Tolerance to Non-Ionising Radiation

- **Reduce mean free path of signal e$^-$:**
  - **Reduce pixel pitch (optimise w.r.t. r.o. speed)**
  - **Improve efficiency of charge collection system (pixel design optimisation)**
  - **Optimise operation temperature**
  - **Investigate annealing possibilities**

- **Improve S/N performance :**
  - **Optimise pixel and r.o. architecture**
  - **Investigate thick epitaxy techno. $\mapsto$ AMS 0.35 OPTO "20 μm" epitaxy option**
  - **Optimise cluster reconstruction algorithms**

- **Equip each detector layer with 2 layers of sensors**

↪ ○ **90 % detection efficiency per layer allows 99 % overall detection efficiency**

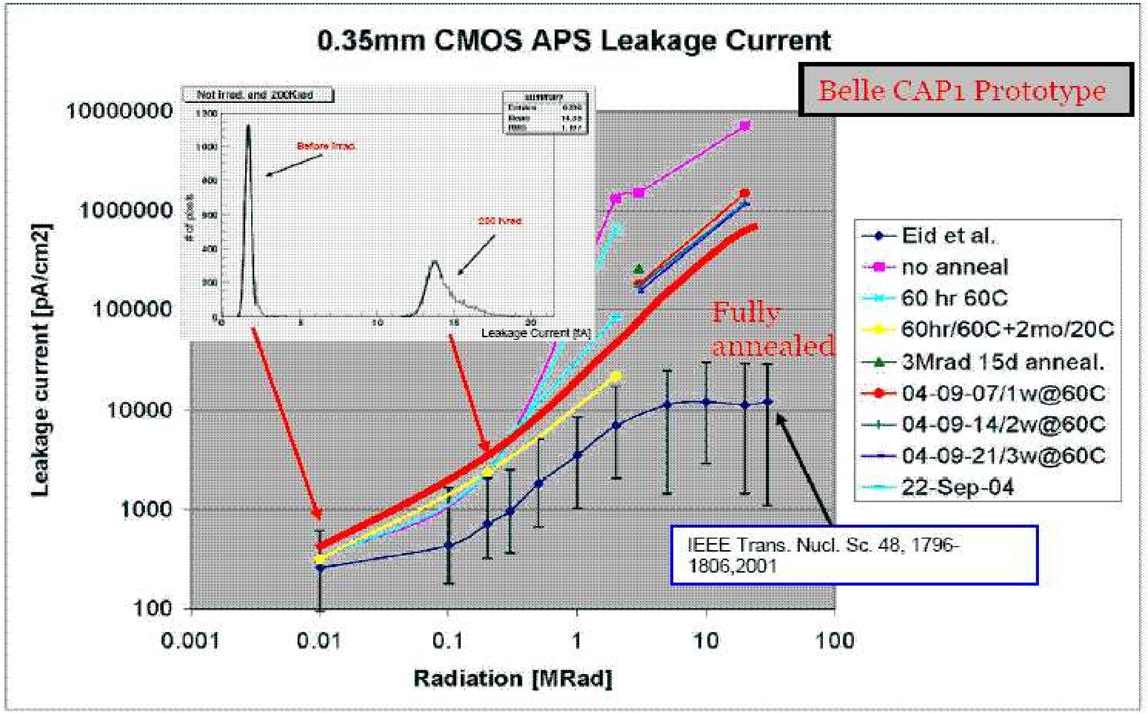
○ **double layer $\mapsto$ track mini-segments from loosely selected clusters $\mapsto$ improved detection efficiency**

  - **Thinning sensors to ultimate thickness ($\sim$ 35 μm) is particularly valuable**
  - **Design mechanical support allowing double sensor layer per detector layer**

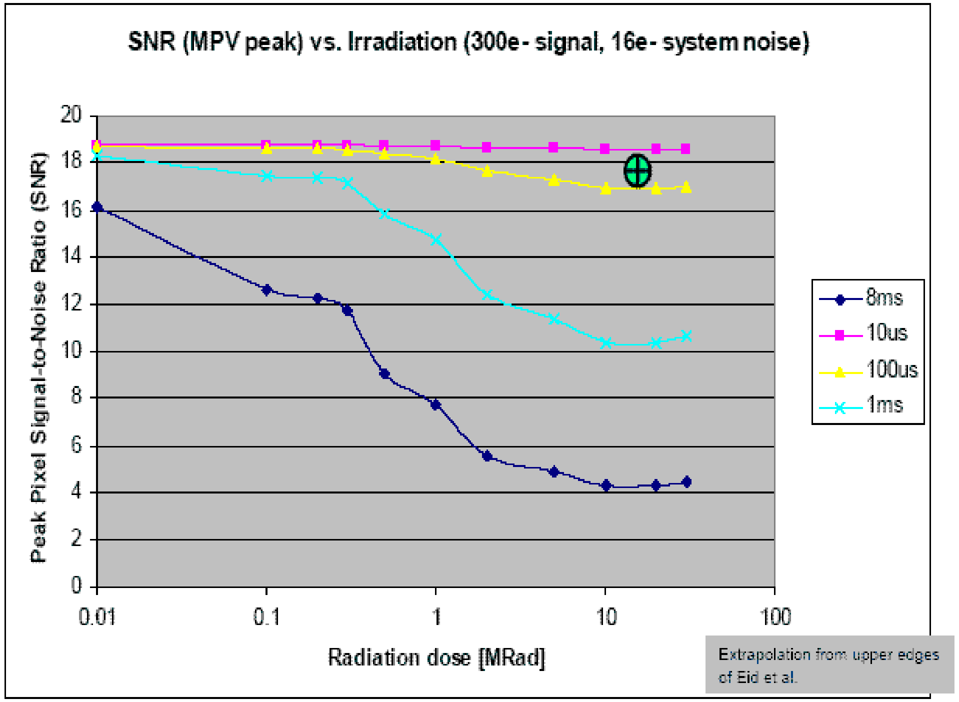
Radiation Tolerance: Ionising Radiation (1/3)

▶ **3 major effects expected from ionising radiation:**

- ◇ Shift of threshold voltages: $\propto$ Nb(holes) created & trapped in gate oxide $\propto$ oxide thickness
  $\hookrightarrow$ aim for $\lesssim$ 10 nm thick oxide ($\sim$ the case for $\leq$ 0.35 μm technologies)
- ◇ Leakage current in NMOS transistors
- ◇ Leakage current in N-channel intertransistors

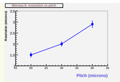


IEEE Trans. Nucl. Sc. 48, 1796-1806,2001



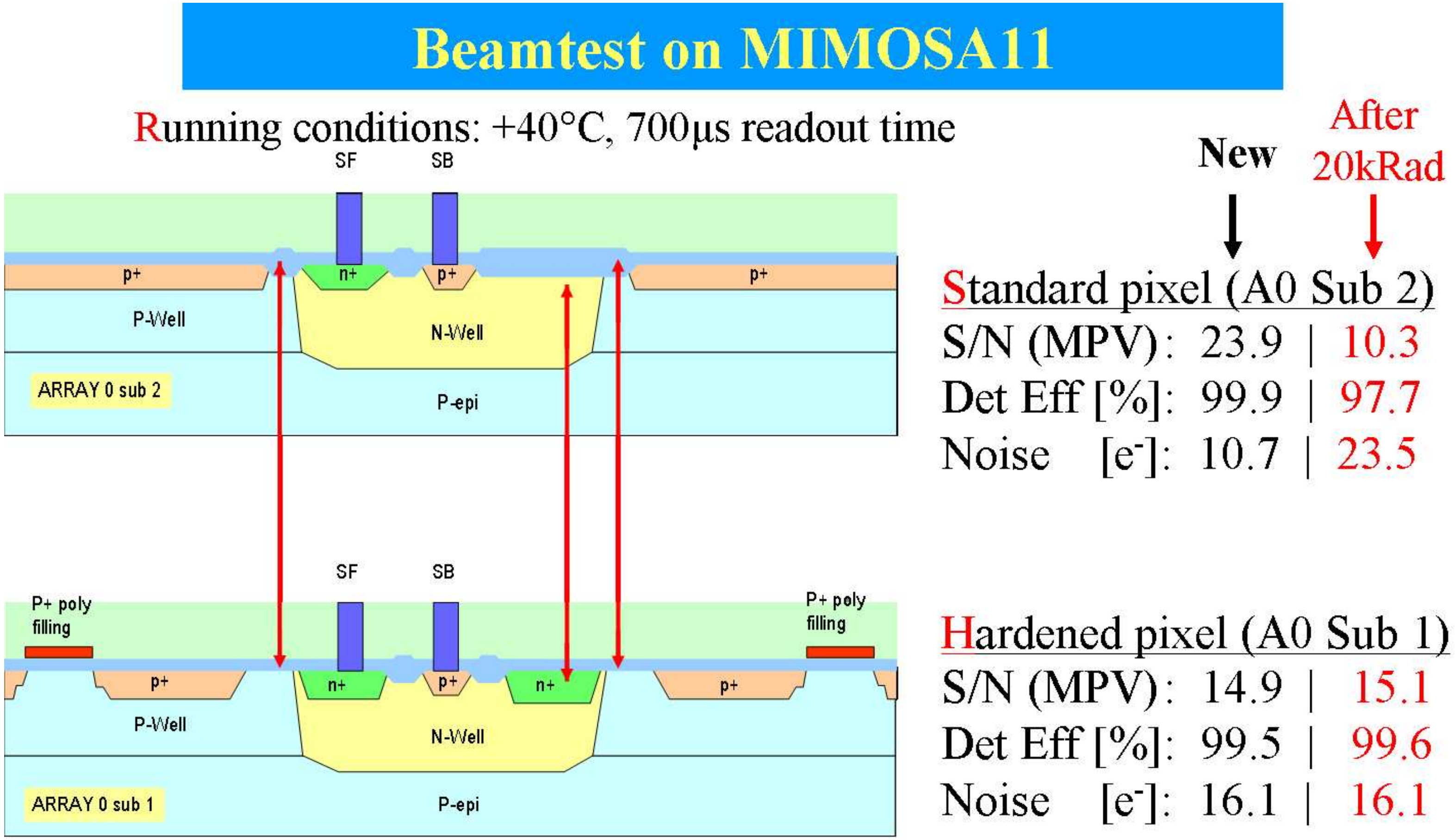
Extrapolation from upper edges of Eid et al.

▶ **Aim for short integration time and for T $\lesssim$ 0°C**



Improving Tolerance to Ionising Radiation (2/3)

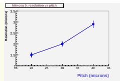
- **Modified pixel design:**
  - **removal of thick oxide nearby the N-well (against charge accumulation**
  - **implantation of P+ guard-ring in polysilicon around N-well (against leakage current)**



Beamtest on MIMOSA11

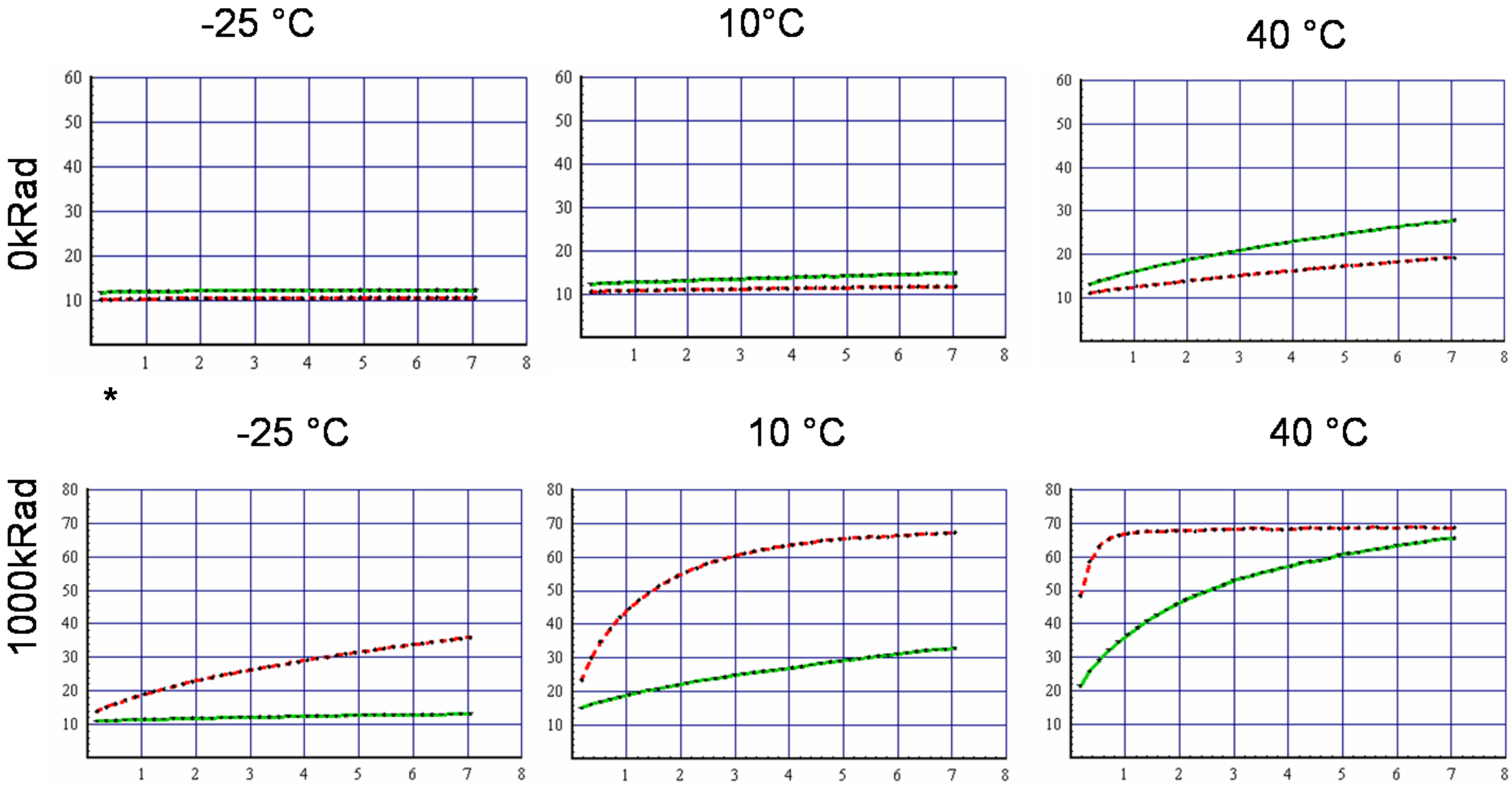
Running conditions: +40°C, 700µs readout time

	New	After 20kRad
Standard pixel (A0 Sub 2)		
S/N (MPV):	23.9	10.3
Det Eff [%]:	99.9	97.7
Noise [e$^-$]:	10.7	23.5
Hardened pixel (A0 Sub 1)		
S/N (MPV):	14.9	15.1
Det Eff [%]:	99.5	99.6
Noise [e$^-$]:	16.1	16.1



- Improved Tolerance to Ionising Radiation (3/3)

- **Noise perfomance of pixel adapted to ionising radiation : Noise (e^- ENC) vs Integration time (ms) for Ordinary and Radiation Tolerant pixels, measured at T = - 25°C, + 10 °C and + 40°C**



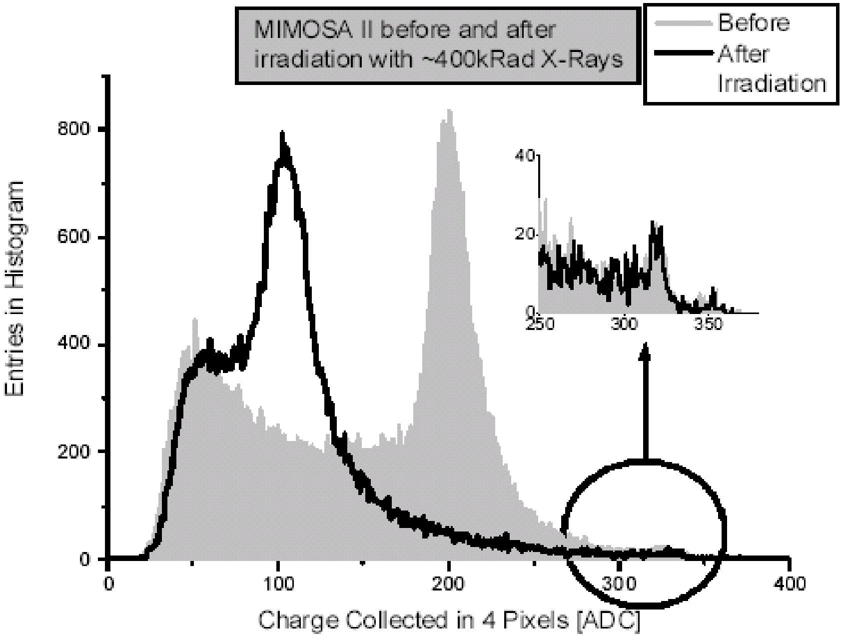
▷▷▷ **1 MRad tolerance demonstrated (esp. at $T < 0^{\circ}$)** ▷▷▷ **Room for improvement**

Technology related Ionising Radiation Effects (1/2)

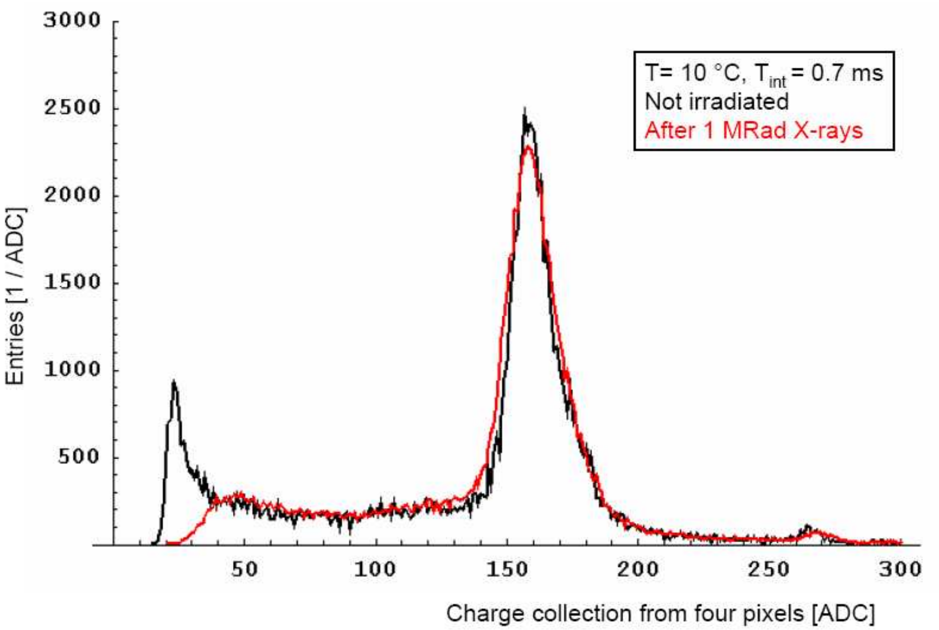
- **Comparison of charge collection efficiency after 10 keV X-Ray irradiation for 2 different technologies**

- **MIMOSA prototypes manufactured in AMI-0.35 and AMS-0.35 OPTO**
  and tested with ^{55}Fe at T = + 10°C before/after irradiation :

⇨AMI-0.35 : 400 kRad , 3.3 ms integration time



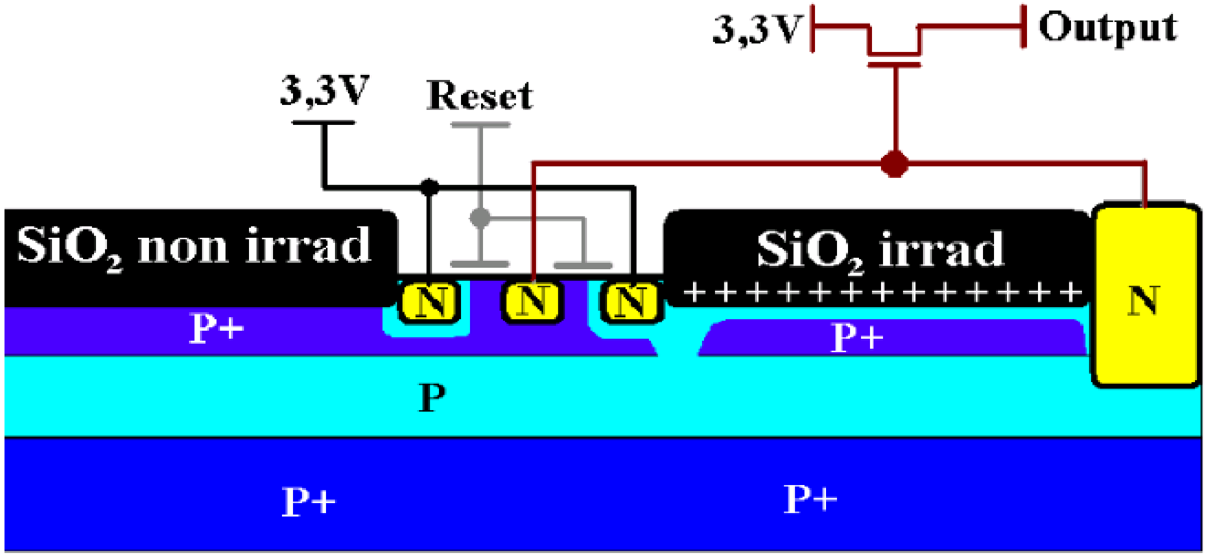
⇨AMS-0.35 OPTO : 1 MRad , 0.7 ms integration time



▷ **AMS-0.35 OPTO sensor does not exhibit any observable drop in charge coll. efficiency after 1 MRad**

Technology related Ionising Radiation Effects (1/2)

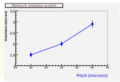
- Charge loss consecutive to ionising radiation seems related to positive oxide charge build-up at Si-SiO$_2$ interfaces ⇛ relatively strong potential depleting P+ coating of N-MOS T
  - ↪ part of the signal electrons get attracted and do not reach the charge collecting diode
- The effect seems technology dependent ⇛ different P+ coating of N-MOS T (?)
  - ↪ not predictible (fabrication parameter)



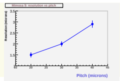
MIMOSA-2 like

Gain: 6.4 e/ADC
LCurrent: 3.6 fA => 31 fA
Noise: 17 e => 21 e

$I_{irr} / I_o = 8.6$
$N_{irr}/N_o = 1.2$



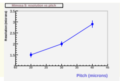
SUMMARY



SUMMARY

- **CMOS sensor technology R&D started in 1999 :**
  - ⇒ **now assessed quite extensively $\rightarrowtail$ attractive tracking/vertexing performances well established**
    - ⇒ **$\sim$ ready to equip high precision tracking detectors (provided rad. levels and r.o. speed are not "extreme")**
      - ⇒ **1st detector made of CMOS sensors should be commissioned in a few years:**
        - ≎ **STAR-HFT : 1) 2008, 2) 2011** ≎ **BELLE-VD ($\lesssim$ 2010 ?)** ≎**EUDET beam telescope : 1) 2007 2) 2008**

- **Wide spectrum of CMOS sensor potential still poorly explored/exploited (e.g. integrated signal processing) :**
  - ● **Strong, growing, R&D community able to undertake the challenge :**
    - ≎ **$\sim$ 10 groups involved in chip design** ≎ **$\gtrsim$ 10 groups concentrating on tests and integration issues**
      - ⇒ **several issues poorly covered $\rightarrowtail$ newcomers ...**
  - ● **Several demanding mid-term applications under way :** ≎ **ILC ($\sim$ 2015)** ≎ **CBM ($\gtrsim$ 2012)** ≎ **etc.**



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⇛ **Main R&D efforts in the coming years:**

◇ **Fast col. // architecture with integ. ADC & sparsification** ◇ **Fab. proc. with feature size $< 0.25\ \mu m$**

◇ **Charge collection systems with improved S/N** ◇ **Improved radiation tolerance (vs T)**

◇ **Complete thinning $\sim 50\ \mu m$ & try $\lesssim 35\ \mu m$** ▷ **Trade-off: P$_{diss.}$ / T$_{oper.}$ / cooling / mat.bud., ...**

▷ ▷ ▷ **Right time to combine & share knowledge & efforts (?)**

$\hookrightarrow$ **several spin-offs in imaging**